U N I V E R S I T A T E A T E H N I C Ă " G H E O R G H E A S A C H I " D I N I A Ş I
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Domeniul: Electronica, Specializarea TST
Disciplina : ___ET__, Anul de studii _4__, Sesiunea _____ / __2019/2020

Homework assignment no. 1

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.55 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.145 mm and use a material with $\varepsilon_r = 2.50$ and $\tan \delta = 0.0110$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 79 mm and height of 67 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 34$ mm to $y_2 = 37$ mm
- bus 2, upper trace from $y_3 = 21$ mm to $y_4 = 53$ mm
- IC1, $x_1 = 29$ mm, $y_1 = 7$ mm
- IC2, $x_2 = 35$ mm, $y_2 = 56$ mm

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Homework assignment no. 2

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.65 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.105 mm and use a material with $\varepsilon_r = 3.40$ and $\tan \delta = 0.0075$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 65 mm and height of 75 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 37$ mm to $y_2 = 47$ mm
- bus 2, upper trace from $y_3 = 51$ mm to $y_4 = 37$ mm
- IC1, $x_1 = 25$ mm, $y_1 = 12$ mm
- IC2, $x_2 = 41$ mm, $y_2 = 69$ mm

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Homework assignment no. 3

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.50 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.145 mm and use a material with $\varepsilon_r = 3.95$ and $\tan \delta = 0.0140$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 75 mm and height of 71 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 26$ mm to $y_2 = 30$ mm
- bus 2, upper trace from $y_3 = 39$ mm to $y_4 = 18$ mm
- IC1, $x_1 = 29$ mm, $y_1 = 6$ mm
- IC2, $x_2 = 35$ mm, $y_2 = 59$ mm

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Homework assignment no. 4

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.70 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.180 mm and use a material with $\varepsilon_r = 4.05$ and $\tan \delta = 0.0170$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 78 mm and height of 69 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 35$ mm to $y_2 = 25$ mm
- bus 2, upper trace from $y_3 = 48$ mm to $y_4 = 14$ mm
- IC1, $x_1 = 27$ mm, $y_1 = 10$ mm
- IC2, $x_2 = 48$ mm, $y_2 = 57$ mm

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Homework assignment no. 5

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.70 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.245 mm and use a material with $\varepsilon_r = 2.10$ and $\tan \delta = 0.0120$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 74 mm and height of 77 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 37$ mm to $y_2 = 30$ mm
- bus 2, upper trace from $y_3 = 49$ mm to $y_4 = 21$ mm
- IC1, $x_1 = 36$ mm, $y_1 = 4$ mm
- IC2, $x_2 = 27$ mm, $y_2 = 70$ mm

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Homework assignment no. 6

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.50 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.110 mm and use a material with $\varepsilon_r = 2.50$ and $\tan \delta = 0.0070$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 64 mm and height of 72 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 37$ mm to $y_2 = 36$ mm
- bus 2, upper trace from $y_3 = 23$ mm to $y_4 = 46$ mm
- IC1, $x_1 = 22$ mm, $y_1 = 12$ mm
- IC2, $x_2 = 24$ mm, $y_2 = 61$ mm

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Homework assignment no. 7

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.70 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.105 mm and use a material with $\varepsilon_r = 4.10$ and $\tan \delta = 0.0155$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 72 mm and height of 70 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 28$ mm to $y_2 = 27$ mm
- bus 2, upper trace from $y_3 = 38$ mm to $y_4 = 13$ mm
- IC1, $x_1 = 30$ mm, $y_1 = 6$ mm
- IC2, $x_2 = 29$ mm, $y_2 = 64$ mm

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Homework assignment no. 8

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.65 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.220 mm and use a material with $\varepsilon_r = 3.45$ and $\tan \delta = 0.0035$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 64 mm and height of 66 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 34$ mm to $y_2 = 24$ mm
- bus 2, upper trace from $y_3 = 25$ mm to $y_4 = 34$ mm
- IC1, $x_1 = 26$ mm, $y_1 = 8$ mm
- IC2, $x_2 = 29$ mm, $y_2 = 61$ mm

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Homework assignment no. 9

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.75 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.125 mm and use a material with $\varepsilon_r = 3.25$ and $\tan \delta = 0.0020$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 74 mm and height of 65 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 42$ mm to $y_2 = 40$ mm
- bus 2, upper trace from $y_3 = 34$ mm to $y_4 = 47$ mm
- IC1, $x_1 = 46$ mm, $y_1 = 4$ mm
- IC2, $x_2 = 38$ mm, $y_2 = 60$ mm

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Homework assignment no. 10

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.65 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.155 mm and use a material with $\varepsilon_r = 3.40$ and $\tan \delta = 0.0065$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 79 mm and height of 64 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 24$ mm to $y_2 = 24$ mm
- bus 2, upper trace from $y_3 = 36$ mm to $y_4 = 10$ mm
- IC1, $x_1 = 32$ mm, $y_1 = 7$ mm
- IC2, $x_2 = 38$ mm, $y_2 = 56$ mm

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Homework assignment no. 11

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.65 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.155 mm and use a material with $\varepsilon_r = 2.45$ and $\tan \delta = 0.0085$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 75 mm and height of 67 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 39$ mm to $y_2 = 33$ mm
- bus 2, upper trace from $y_3 = 27$ mm to $y_4 = 44$ mm
- IC1, $x_1 = 26$ mm, $y_1 = 13$ mm
- IC2, $x_2 = 27$ mm, $y_2 = 56$ mm

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Homework assignment no. 12

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.50 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.180 mm and use a material with $\varepsilon_r = 3.65$ and $\tan \delta = 0.0095$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 67 mm and height of 75 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 35$ mm to $y_2 = 44$ mm
- bus 2, upper trace from $y_3 = 43$ mm to $y_4 = 33$ mm
- IC1, $x_1 = 41$ mm, $y_1 = 4$ mm
- IC2, $x_2 = 29$ mm, $y_2 = 68$ mm

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Homework assignment no. 13

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.75 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.105 mm and use a material with $\varepsilon_r = 3.65$ and $\tan \delta = 0.0190$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 77 mm and height of 78 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 46$ mm to $y_2 = 30$ mm
- bus 2, upper trace from $y_3 = 33$ mm to $y_4 = 49$ mm
- IC1, $x_1 = 47$ mm, $y_1 = 14$ mm
- IC2, $x_2 = 34$ mm, $y_2 = 67$ mm

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Homework assignment no. 14

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.65 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.185 mm and use a material with $\varepsilon_r = 4.15$ and $\tan \delta = 0.0045$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 66 mm and height of 75 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 41$ mm to $y_2 = 42$ mm
- bus 2, upper trace from $y_3 = 33$ mm to $y_4 = 50$ mm
- IC1, $x_1 = 34$ mm, $y_1 = 8$ mm
- IC2, $x_2 = 37$ mm, $y_2 = 69$ mm

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Homework assignment no. 15

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.65 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.110 mm and use a material with $\varepsilon_r = 2.40$ and $\tan \delta = 0.0150$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 79 mm and height of 62 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 32$ mm to $y_2 = 24$ mm
- bus 2, upper trace from $y_3 = 23$ mm to $y_4 = 35$ mm
- IC1, $x_1 = 48$ mm, $y_1 = 11$ mm
- IC2, $x_2 = 37$ mm, $y_2 = 54$ mm

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Homework assignment no. 16

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.60 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.240 mm and use a material with $\varepsilon_r = 2.70$ and $\tan \delta = 0.0185$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 72 mm and height of 76 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 47$ mm to $y_2 = 33$ mm
- bus 2, upper trace from $y_3 = 34$ mm to $y_4 = 47$ mm
- IC1, $x_1 = 31$ mm, $y_1 = 8$ mm
- IC2, $x_2 = 44$ mm, $y_2 = 65$ mm

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Homework assignment no. 17

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.70 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.190 mm and use a material with $\varepsilon_r = 4.00$ and $\tan \delta = 0.0175$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 76 mm and height of 64 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 28$ mm to $y_2 = 23$ mm
- bus 2, upper trace from $y_3 = 38$ mm to $y_4 = 11$ mm
- IC1, $x_1 = 40$ mm, $y_1 = 8$ mm
- IC2, $x_2 = 49$ mm, $y_2 = 53$ mm

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Homework assignment no. 18

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.50 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.140 mm and use a material with $\varepsilon_r = 2.75$ and $\tan \delta = 0.0120$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 71 mm and height of 61 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 34$ mm to $y_2 = 35$ mm
- bus 2, upper trace from $y_3 = 26$ mm to $y_4 = 46$ mm
- IC1, $x_1 = 31$ mm, $y_1 = 4$ mm
- IC2, $x_2 = 28$ mm, $y_2 = 50$ mm

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H o m e w o r k a s s i g n m e n t n o . 1 9

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.55 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.230 mm and use a material with $\varepsilon_r = 3.15$ and $\tan \delta = 0.0040$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 71 mm and height of 60 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 23$ mm to $y_2 = 33$ mm
- bus 2, upper trace from $y_3 = 31$ mm to $y_4 = 24$ mm
- IC1, $x_1 = 31$ mm, $y_1 = 8$ mm
- IC2, $x_2 = 26$ mm, $y_2 = 55$ mm

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H o m e w o r k a s s i g n m e n t n o . 2 0

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.75 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.180 mm and use a material with $\varepsilon_r = 3.50$ and $\tan \delta = 0.0030$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 74 mm and height of 72 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 38$ mm to $y_2 = 37$ mm
- bus 2, upper trace from $y_3 = 25$ mm to $y_4 = 49$ mm
- IC1, $x_1 = 37$ mm, $y_1 = 13$ mm
- IC2, $x_2 = 41$ mm, $y_2 = 62$ mm

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Homework assignment no. 21

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.50 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.175 mm and use a material with $\varepsilon_r = 3.35$ and $\tan \delta = 0.0135$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 62 mm and height of 78 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 32$ mm to $y_2 = 42$ mm
- bus 2, upper trace from $y_3 = 41$ mm to $y_4 = 30$ mm
- IC1, $x_1 = 33$ mm, $y_1 = 4$ mm
- IC2, $x_2 = 33$ mm, $y_2 = 62$ mm

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Homework assignment no. 22

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.65 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.220 mm and use a material with $\varepsilon_r = 3.95$ and $\tan \delta = 0.0040$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 61 mm and height of 71 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 33$ mm to $y_2 = 43$ mm
- bus 2, upper trace from $y_3 = 46$ mm to $y_4 = 34$ mm
- IC1, $x_1 = 22$ mm, $y_1 = 8$ mm
- IC2, $x_2 = 36$ mm, $y_2 = 65$ mm

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Homework assignment no. 23

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.55 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.130 mm and use a material with $\varepsilon_r = 3.65$ and $\tan \delta = 0.0060$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 63 mm and height of 66 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 35$ mm to $y_2 = 34$ mm
- bus 2, upper trace from $y_3 = 22$ mm to $y_4 = 52$ mm
- IC1, $x_1 = 25$ mm, $y_1 = 4$ mm
- IC2, $x_2 = 25$ mm, $y_2 = 53$ mm

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Homework assignment no. 24

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.55 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.115 mm and use a material with $\varepsilon_r = 2.35$ and $\tan \delta = 0.0115$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 75 mm and height of 77 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 27$ mm to $y_2 = 46$ mm
- bus 2, upper trace from $y_3 = 36$ mm to $y_4 = 39$ mm
- IC1, $x_1 = 29$ mm, $y_1 = 6$ mm
- IC2, $x_2 = 35$ mm, $y_2 = 66$ mm

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Homework assignment no. 25

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.70 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.190 mm and use a material with $\varepsilon_r = 3.85$ and $\tan \delta = 0.0170$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 61 mm and height of 65 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 25$ mm to $y_2 = 29$ mm
- bus 2, upper trace from $y_3 = 33$ mm to $y_4 = 22$ mm
- IC1, $x_1 = 29$ mm, $y_1 = 5$ mm
- IC2, $x_2 = 33$ mm, $y_2 = 59$ mm

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Homework assignment no. 26

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.60 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.215 mm and use a material with $\varepsilon_r = 3.35$ and $\tan \delta = 0.0160$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 70 mm and height of 75 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 32$ mm to $y_2 = 44$ mm
- bus 2, upper trace from $y_3 = 44$ mm to $y_4 = 32$ mm
- IC1, $x_1 = 39$ mm, $y_1 = 4$ mm
- IC2, $x_2 = 31$ mm, $y_2 = 62$ mm

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Homework assignment no. 27

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.75 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.110 mm and use a material with $\varepsilon_r = 3.35$ and $\tan \delta = 0.0085$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 60 mm and height of 79 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 39$ mm to $y_2 = 35$ mm
- bus 2, upper trace from $y_3 = 47$ mm to $y_4 = 27$ mm
- IC1, $x_1 = 32$ mm, $y_1 = 12$ mm
- IC2, $x_2 = 26$ mm, $y_2 = 66$ mm

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Homework assignment no. 28

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.65 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.140 mm and use a material with $\varepsilon_r = 2.45$ and $\tan \delta = 0.0180$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 75 mm and height of 77 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 47$ mm to $y_2 = 37$ mm
- bus 2, upper trace from $y_3 = 38$ mm to $y_4 = 49$ mm
- IC1, $x_1 = 32$ mm, $y_1 = 12$ mm
- IC2, $x_2 = 31$ mm, $y_2 = 71$ mm

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H o m e w o r k a s s i g n m e n t n o . 2 9

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.50 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.180 mm and use a material with $\varepsilon_r = 2.10$ and $\tan \delta = 0.0120$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 74 mm and height of 64 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 24$ mm to $y_2 = 24$ mm
- bus 2, upper trace from $y_3 = 32$ mm to $y_4 = 16$ mm
- IC1, $x_1 = 33$ mm, $y_1 = 6$ mm
- IC2, $x_2 = 36$ mm, $y_2 = 60$ mm

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H o m e w o r k a s s i g n m e n t n o . 3 0

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.65 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.150 mm and use a material with $\varepsilon_r = 2.70$ and $\tan \delta = 0.0085$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 66 mm and height of 73 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 33$ mm to $y_2 = 39$ mm
- bus 2, upper trace from $y_3 = 47$ mm to $y_4 = 26$ mm
- IC1, $x_1 = 23$ mm, $y_1 = 9$ mm
- IC2, $x_2 = 40$ mm, $y_2 = 59$ mm

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Homework assignment no. 31

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.55 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.200 mm and use a material with $\varepsilon_r = 4.30$ and $\tan \delta = 0.0185$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 78 mm and height of 65 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 25$ mm to $y_2 = 27$ mm
- bus 2, upper trace from $y_3 = 33$ mm to $y_4 = 19$ mm
- IC1, $x_1 = 36$ mm, $y_1 = 8$ mm
- IC2, $x_2 = 35$ mm, $y_2 = 58$ mm

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Homework assignment no. 32

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.60 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.130 mm and use a material with $\varepsilon_r = 2.20$ and $\tan \delta = 0.0070$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 78 mm and height of 67 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 27$ mm to $y_2 = 42$ mm
- bus 2, upper trace from $y_3 = 38$ mm to $y_4 = 31$ mm
- IC1, $x_1 = 27$ mm, $y_1 = 12$ mm
- IC2, $x_2 = 47$ mm, $y_2 = 54$ mm

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Homework assignment no. 33

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.50 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.245 mm and use a material with $\varepsilon_r = 2.95$ and $\tan \delta = 0.0170$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 76 mm and height of 74 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 27$ mm to $y_2 = 28$ mm
- bus 2, upper trace from $y_3 = 39$ mm to $y_4 = 18$ mm
- IC1, $x_1 = 49$ mm, $y_1 = 8$ mm
- IC2, $x_2 = 31$ mm, $y_2 = 68$ mm

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Homework assignment no. 34

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.65 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.140 mm and use a material with $\varepsilon_r = 2.15$ and $\tan \delta = 0.0185$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 79 mm and height of 65 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 23$ mm to $y_2 = 34$ mm
- bus 2, upper trace from $y_3 = 33$ mm to $y_4 = 25$ mm
- IC1, $x_1 = 42$ mm, $y_1 = 7$ mm
- IC2, $x_2 = 32$ mm, $y_2 = 53$ mm

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Homework assignment no. 35

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.70 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.245 mm and use a material with $\varepsilon_r = 2.95$ and $\tan \delta = 0.0020$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 75 mm and height of 63 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 24$ mm to $y_2 = 23$ mm
- bus 2, upper trace from $y_3 = 33$ mm to $y_4 = 12$ mm
- IC1, $x_1 = 42$ mm, $y_1 = 8$ mm
- IC2, $x_2 = 44$ mm, $y_2 = 50$ mm

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Homework assignment no. 36

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.60 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.185 mm and use a material with $\varepsilon_r = 2.50$ and $\tan \delta = 0.0080$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 76 mm and height of 78 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 46$ mm to $y_2 = 42$ mm
- bus 2, upper trace from $y_3 = 34$ mm to $y_4 = 52$ mm
- IC1, $x_1 = 29$ mm, $y_1 = 9$ mm
- IC2, $x_2 = 33$ mm, $y_2 = 69$ mm

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Homework assignment no. 37

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.55 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.155 mm and use a material with $\varepsilon_r = 4.20$ and $\tan \delta = 0.0150$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 68 mm and height of 65 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 34$ mm to $y_2 = 25$ mm
- bus 2, upper trace from $y_3 = 22$ mm to $y_4 = 36$ mm
- IC1, $x_1 = 30$ mm, $y_1 = 7$ mm
- IC2, $x_2 = 24$ mm, $y_2 = 53$ mm

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Homework assignment no. 38

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.60 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.145 mm and use a material with $\varepsilon_r = 3.55$ and $\tan \delta = 0.0025$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 72 mm and height of 68 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 29$ mm to $y_2 = 34$ mm
- bus 2, upper trace from $y_3 = 42$ mm to $y_4 = 22$ mm
- IC1, $x_1 = 27$ mm, $y_1 = 8$ mm
- IC2, $x_2 = 46$ mm, $y_2 = 59$ mm

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H o m e w o r k a s s i g n m e n t n o . 3 9

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.75 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.190 mm and use a material with $\varepsilon_r = 3.70$ and $\tan \delta = 0.0030$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 72 mm and height of 77 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 36$ mm to $y_2 = 40$ mm
- bus 2, upper trace from $y_3 = 48$ mm to $y_4 = 31$ mm
- IC1, $x_1 = 31$ mm, $y_1 = 11$ mm
- IC2, $x_2 = 35$ mm, $y_2 = 69$ mm

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H o m e w o r k a s s i g n m e n t n o . 4 0

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.50 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.150 mm and use a material with $\varepsilon_r = 4.25$ and $\tan \delta = 0.0075$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 63 mm and height of 60 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 29$ mm to $y_2 = 23$ mm
- bus 2, upper trace from $y_3 = 39$ mm to $y_4 = 12$ mm
- IC1, $x_1 = 30$ mm, $y_1 = 11$ mm
- IC2, $x_2 = 25$ mm, $y_2 = 56$ mm

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Homework assignment no. 41

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.70 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.180 mm and use a material with $\varepsilon_r = 2.75$ and $\tan \delta = 0.0175$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 73 mm and height of 60 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 29$ mm to $y_2 = 34$ mm
- bus 2, upper trace from $y_3 = 39$ mm to $y_4 = 23$ mm
- IC1, $x_1 = 45$ mm, $y_1 = 4$ mm
- IC2, $x_2 = 37$ mm, $y_2 = 56$ mm

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Homework assignment no. 42

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.55 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.195 mm and use a material with $\varepsilon_r = 2.55$ and $\tan \delta = 0.0195$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 74 mm and height of 79 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 48$ mm to $y_2 = 46$ mm
- bus 2, upper trace from $y_3 = 36$ mm to $y_4 = 56$ mm
- IC1, $x_1 = 38$ mm, $y_1 = 13$ mm
- IC2, $x_2 = 36$ mm, $y_2 = 70$ mm

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Homework assignment no. 43

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.55 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.130 mm and use a material with $\varepsilon_r = 3.90$ and $\tan \delta = 0.0040$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 66 mm and height of 74 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 46$ mm to $y_2 = 27$ mm
- bus 2, upper trace from $y_3 = 35$ mm to $y_4 = 35$ mm
- IC1, $x_1 = 38$ mm, $y_1 = 4$ mm
- IC2, $x_2 = 41$ mm, $y_2 = 70$ mm

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Homework assignment no. 44

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.70 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.155 mm and use a material with $\varepsilon_r = 3.25$ and $\tan \delta = 0.0115$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 61 mm and height of 71 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 25$ mm to $y_2 = 36$ mm
- bus 2, upper trace from $y_3 = 35$ mm to $y_4 = 29$ mm
- IC1, $x_1 = 35$ mm, $y_1 = 9$ mm
- IC2, $x_2 = 31$ mm, $y_2 = 67$ mm

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Homework assignment no. 45

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.75 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.170 mm and use a material with $\varepsilon_r = 4.35$ and $\tan \delta = 0.0115$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 77 mm and height of 73 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 39$ mm to $y_2 = 26$ mm
- bus 2, upper trace from $y_3 = 32$ mm to $y_4 = 33$ mm
- IC1, $x_1 = 45$ mm, $y_1 = 9$ mm
- IC2, $x_2 = 49$ mm, $y_2 = 58$ mm

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Homework assignment no. 46

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.65 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.170 mm and use a material with $\varepsilon_r = 2.50$ and $\tan \delta = 0.0030$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 76 mm and height of 79 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 49$ mm to $y_2 = 42$ mm
- bus 2, upper trace from $y_3 = 40$ mm to $y_4 = 51$ mm
- IC1, $x_1 = 30$ mm, $y_1 = 14$ mm
- IC2, $x_2 = 29$ mm, $y_2 = 63$ mm

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Homework assignment no. 47

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.75 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.175 mm and use a material with $\varepsilon_r = 2.40$ and $\tan \delta = 0.0195$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the top layer (M1)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 63 mm and height of 66 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-down corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 30$ mm to $y_2 = 32$ mm
- bus 2, upper trace from $y_3 = 41$ mm to $y_4 = 20$ mm
- IC1, $x_1 = 38$ mm, $y_1 = 12$ mm
- IC2, $x_2 = 33$ mm, $y_2 = 55$ mm

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Homework assignment no. 48

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.60 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.240 mm and use a material with $\varepsilon_r = 3.30$ and $\tan \delta = 0.0070$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 67 mm and height of 62 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the right-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 31$ mm to $y_2 = 37$ mm
- bus 2, upper trace from $y_3 = 40$ mm to $y_4 = 24$ mm
- IC1, $x_1 = 28$ mm, $y_1 = 7$ mm
- IC2, $x_2 = 36$ mm, $y_2 = 58$ mm

U N I V E R S I T A T E A T E H N I C Ă " G H E O R G H E A S A C H I " D I N I A Ş I
Facultatea / Departamentul: Electronica,Telecomunicatii si Ingineria Informatiei
Domeniul: Electronica, Specializarea TST
Disciplina : ___ET__, Anul de studii _4__, Sesiunea _____ / __2019/2020

Homework assignment no. 49

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.75 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.140 mm and use a material with $\varepsilon_r = 2.65$ and $\tan \delta = 0.0135$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 60 mm and height of 71 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 35$ mm to $y_2 = 28$ mm
- bus 2, upper trace from $y_3 = 44$ mm to $y_4 = 21$ mm
- IC1, $x_1 = 38$ mm, $y_1 = 6$ mm
- IC2, $x_2 = 29$ mm, $y_2 = 60$ mm

U N I V E R S I T A T E A T E H N I C Ă " G H E O R G H E A S A C H I " D I N I A Ş I
Facultatea / Departamentul: Electronica,Telecomunicatii si Ingineria Informatiei
Domeniul: Electronica, Specializarea TST
Disciplina : ___ET__, Anul de studii _4__, Sesiunea _____ / __2019/2020

Homework assignment no. 50

Design a PCB using this technology:

- Use 4 metal layers, each having the conductivity $\sigma = 5.50 \cdot 10^7$ S/m (M1 to M4)
- All dielectric layers have the thickness of 0.215 mm and use a material with $\varepsilon_r = 3.80$ and $\tan \delta = 0.0065$
- The ground and power planes are placed on the intermediate metal layers (M2 and M3)
- Signal traces are on the bottom layer (M4)
- Trace width should be computed to provide a 50Ω characteristic impedance (rounded to closest 0.05 mm multiple: e.g. 0.200, 0.250, 0.300, 0.350 ...), trace thickness is 0.035mm

The PCB has a width of 68 mm and height of 75 mm. In every corner a 5 mm square must be left metal free (all layers!) for screw holes. The external power supply is connected on two pads in the left-up corner. On the PCB you will have two signal buses, 3 traces each (from one side of the PCB to the opposite side, the traces have the same width and are separated by the same distance - equal to the trace width) and two IC (two pads each for DC power supply connection) as follows:

- bus 1, upper trace from $y_1 = 44$ mm to $y_2 = 43$ mm
- bus 2, upper trace from $y_3 = 35$ mm to $y_4 = 56$ mm
- IC1, $x_1 = 37$ mm, $y_1 = 13$ mm
- IC2, $x_2 = 28$ mm, $y_2 = 60$ mm