Microwave amplifier design

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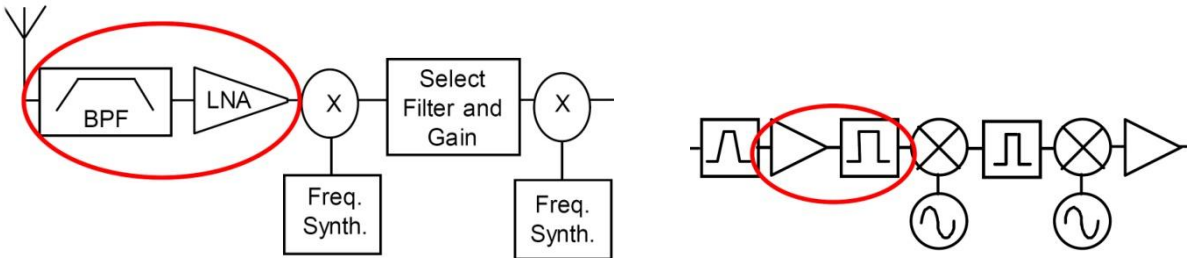
Important Note 1. There is no "magic information" hidden in the middle of this document. You have to go through it step by step without "jumping" in search of the important area.

Important Note 2. Even if your experience with digital data has convinced you that an image contains as much information as a thousand pages of text, try not to skip the small black-on-white objects called "letters" between the various pictures in the document.

1. Assignment.

We design the input stage is from an RF receiver, which typically contains one or two bandpass filters and a low noise amplifier. Although the position and number of filters vary, there is generally a filter before the amplifier to limit the bandwidth of the signal applied to it and a filter after the amplifier.



Your assignment is a low-noise multi-stage transistor amplifier required to provide a power gain of **G[dB]** and a noise factor of **F[dB]** at the design frequency **f[GHz]**. At the output of the amplifier insert a **Nth** order bandpass filter with fractional bandwidth of the passband **B[%]** around the design frequency. The amplifier must work with a 50Ω source and 50Ω load.

The numerical results in this document are for a sample assignment: an amplifier with a gain of (minimum) 20dB, and a noise factor of (maximum) 1dB, at the frequency of 5GHz, followed or preceded by a 4th order bandpass filter with fractional bandwidth of the passband of 10%.

2. Observations about the assignment data

A few (important) observations about the individual assignment data:

- Even if for certain particular assignments it would be possible to use a single transistor to achieve the required gain, this solution is **not** allowed (multi-stage amplifier), and is generally not recommended because it usually involves designing at the theoretical limit for performance, an approach that backfires during a (eventual) practical implementation.
- Frequency related data (including filter characteristics, bandwidth) must be interpreted absolutely and accurately. The other parameters represent lower performance limits that must be met relatively (from a practical point of view). An amplifier with a higher gain is better, an amplifier with a lower noise is better. As a result, the gain can be targeted (and it is recommended to be) higher than in the assignment, without exaggerating. For example, of all the 20dB amplifiers, the one with a real gain of 22dB will be better, the one with a gain of 25dB will be even better if it can be obtained with the same investment, but it is useless and

impractical to target a gain of 40dB using twice as many components, consuming twice as much power or twice the space on the circuit board.

- Regarding the noise factor, the rule is simple, the smaller the better. For example, of all the 20dB amplifiers in the world, the best is the one with the lowest noise. After choosing the transistor, it also makes great sense to get the lowest possible noise from that transistor. In practice, it is not advisable to choose a more expensive component to exceed the design parameters, even if that component is more efficient, but after a component has been chosen, noise optimization (getting as much performance possible with the same cost) is always useful.

3. Separation of the design parameters on the 2 amplification stages

also see: L8/2021, S 175-179.

We use Friis formula with its main effects:

- it's essential that the first stage is as **noiseless** as possible even if that means sacrificing power gain
- the following stages can be optimized for **power gain** as their noise figure will have a lower influence on the overall noise

$$F_{cas} = F_1 + \frac{1}{G_1}(F_2 - 1) \text{(linear scale!)} \quad G_{cas} = G_1 \cdot G_2 \text{(linear scale) or} \quad G_{cas}[dB] = G_1[dB] + G_2[dB]$$

For the sample assignment F = 1dB, G = 20dB we can separate the design parameters between the two stages as:

- first/input stage: F1 = 0.7 dB, G1 = 9 dB
- second/output stage: F2 = 1.2 dB, G2 = 13 dB

Remember that we have 2 equations (Friis) and 4 unknowns (F1,G1,F2,G2) so we estimate those unknowns then we check (repeatedly, until correct) that they verify Friis formula:

$$F_1 = 10^{\frac{F_1[dB]}{10}} = 10^{0.07} = 1.175,\ F_2 = 10^{\frac{F_2[dB]}{10}} = 10^{0.12} = 1.318,$$

$$F_{cas} = F_1 + \frac{1}{G_1}(F_2 - 1) = 1.215,\ \ F_{cas} = 10 \cdot \log(1.215) = 0.846\ dB,$$

$$G_1 = 10^{\frac{G_1[dB]}{10}} = 10^{0.9} = 7.943,\ G_2 = 10^{\frac{G_2[dB]}{10}} = 10^{1.3} = 19.953,$$

$$G_{cas} = G_1 \cdot G_2 = 158.49,\ G_{cas} = 10 \cdot \log(158.49) = 22\ dB$$

This choice meets the target for the assignment, with the appropriate reserve/design margin required to account for subsequent problems (additional losses on the lines, the influence of parasitic elements on noise, etc.):

- F = 0.85 dB, G = 22 dB
- $G = G_{design} + \Delta G$
- $F = F_{design} - \Delta F$

4. Selection of the number of transistor types

The assignment requires that we use at least two transistors for the amplifier, but we must decide whether to use the same transistor type in both stages or to use two different transistor types. The two stages have different requirements which suggests the use of two different types, a low noise transistor, followed by a higher gain transistor (this is the recommended selection that brings an extra point to the project grade). If this is the case we should be looking for two different transistors:

- first/input stage: F1 (max) = 0.7 dB, G1 (min) = 9 dB
- second/output stage: F2 (max) = 1.2 dB, G2 (min) = 13 dB

However, in the current document, the first option is chosen, namely the use of the same transistor for both amplification stages. This is done for concision of the document and to avoid adding a supplemental transistor to the list of prohibited/penalized components (NE 71084, ATF 34143). The transistor we choose must meet requirements for both stages:

- first/second stage: F = min (F1,F2) = 0.7 dB, G = max(G1,G2) = 13 dB

5. Selection of the transistor(s)

also see Lab3/2021 pt. 1

Important Note 3. Choosing a suitable transistor is a time consuming process, multiple attempts are necessary until the discovery of a suitable component. There is no ideal component usable at any frequency/assignment, forcing the students to apply the search procedure is the reason behind the existence of the prohibited/penalized components.

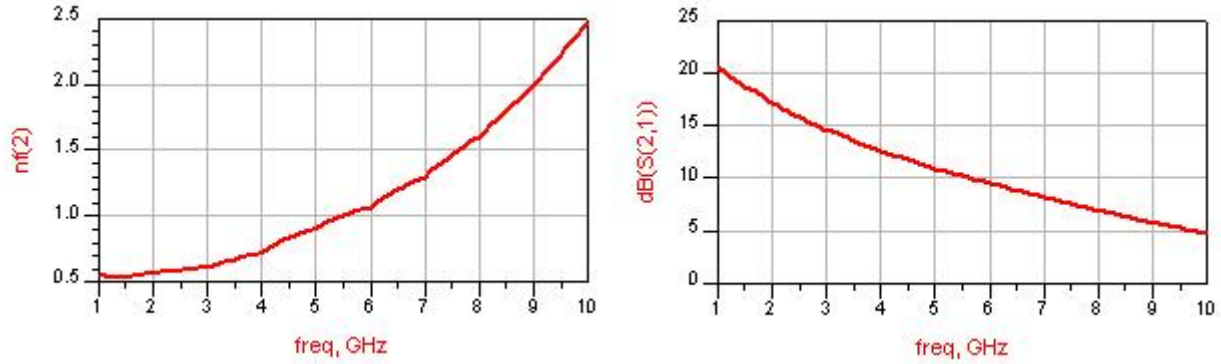
The choice of a particular transistor is controlled by its ability to provide the gain and noise factor at the design frequency. The type of transistor is a first parameter that must be estimated. Currently, bipolar Si based transistors have operating frequencies of up to 2-2.4GHz and higher noise, being designed for use in commercial, unpretentious, low power GSM / wireless applications. Unipolar transistors (usually based on GaAs) have higher operating frequencies (ten/tens of GHz), low noise, but are sensitive to overvoltages/overcurrents and are more complicated to control in direct current (bias). However new technologies like Silicon Germanium Carbon (SiGe:C) might change this conclusion.

In principle, it is recommended to start from the selection guide (one of the first pages in any written component catalog) as it lists some of the key values of those components. A first step is to select "Low Noise" transistors list, as power transistors, general purpose or pulse operation transistors are not suitable for this design.

Low Noise pHEMTs (Typical Specifications @ 25°C Case Temperature)

Part Number	Gate Width (μm)	Frequency Range (GHz)	Test Freq. (GHz)	V_{dd} (V)	I_{dd} (mA)	NF_o (dB)	G_a (dB)	OIP3 (dBm)	$P_{1\,dB}$ (dBm)	Package
ATF-33143	1600	0.45 - 6	2	4	80	0.5	15.0	33.5	+22	SOT-343 (SC-70)
ATF-331M4	1600	0.45 - 6	2	4	60	0.6	15.0	31	+19	MiniPak[2]
ATF-34143	800	0.45 - 6	2	4	60	0.5	17.5	31.5	+20	SOT-343 (SC-70)
ATF-35143	400	0.45 - 6	2	2	15	0.4	18.0	21	+10	SOT-343 (SC-70)
ATF-38143	800	0.45 - 6	2	2	10	0.4	16.0	22	+12	SOT-343 (SC-70)
ATF-36077	200	1.5 - 18	12	1.5	10	0.5	12.0	—	+5	70 mil SM
ATF-36163	200	1.5 - 18	12	1.5	15	1.2	10.0	—	+5	SOT-363 (SC-70)

Above is an example of the selection guide for transistors from Agilent/Avago/HP. Not all selection guides show the recommended "Frequency Range", but if it exists, the manufacturer's indication may be taken into account. Instead, the "Test Frequency", minimum noise factor (NF_0), and associated gain (G_a) (at that test frequency) are always present. We must remember that the parameters that interest us vary with the frequency, typically the gain expressed in dB decreases linearly with the frequency and the noise factor expressed in dB increases exponentially with the frequency (under normal use conditions – below is the typical variation for ATF 34143). Usually, an extrapolation from the test frequency should be made to estimate typical values at the design frequency.



For the sample assignment, we can start from information from the selection guide/datasheet, so from NF = 0.5dB, G = 17.5dB at 2GHz, we can estimate a performance of about NF = 0.7÷0.8dB and G = 14÷15dB at 5GHz, at 4V/60mA bias.

Important Note 4. Remember that the signal performance strongly depends on the bias point, so it is recommended, after choosing the transistor, to look for the optimal bias point for the current application. Usually low voltage/low current biases offer less noise but also less gain, of course with the decrease of current and power that can be handled by that particular transistor.

It is advisable to obtain (Google) the complete datasheet for the candidate transistor. For example for ATF34143 (Avago) from the datasheet we can extract the following details for operation at 5GHz:

- bias point of 4V Vds, 60mA Ids offers Fmin = 0.67dB, MSG = 15.23dB
- bias point of 3V Vds, 20mA Ids offers Fmin = 0.54dB, MSG = 14.25dB

We choose to continue with a bias point of 3V/20mA Vds/Ids for both amplification stages. In real situations, if increasing the complexity of the bias circuit is not a problem, different bias points for the first and second stages can be chosen.

Important Note 5. The fulfillment of separate noise/gain conditions does not necessarily mean that the application as a whole will be fully satisfied. For example, a low noise amplifier involves **simultaneously** fulfilling several conditions: gain/noise/stability/realizability of components needed for impedance matching. It might be necessary to return to the transistor selection phase if later the chosen component proves unsuitable.

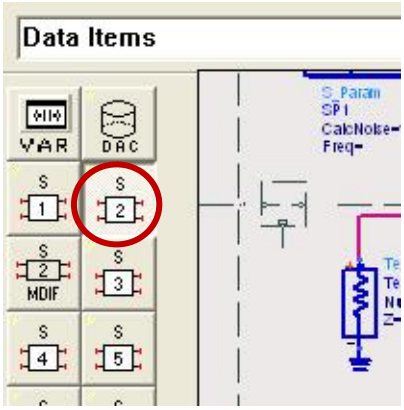
6. Model data for transistors

In order to use the transistor in ADS it is necessary to obtain the model data for the transistor. For ATF34143, the complete ADS model of the transistor is available for download (including case parasitics, layout). We will not use this model because:

- Such models are not always available. For Avago ATF34143 this is due to the company's history: HP = HP + Agilent, Agilent = Agilent + Keysight + Avago
- The complete ADS model is an integral component model and in order to be used it must be properly biased, which goes beyond the scope of the current project assignment. In real situations, however, this would be an advantage (correct modeling of the dependence signal performance/bias).

What you really need for a device is the list of S and noise parameters at different frequencies. The values can be obtained from a traditional **datasheet** or can be obtained as ready to use **files** from the manufacturer's **website**. The standard format is called Touchstone and consists of clear text listings of the complex values in the form of a module/argument. The format is not difficult to interpret or modify/create if you cannot find the **s2p file**. The typical extension for transistors is "*.s2p" (2 represents the number of ports, a diode will have "*.s1p" files for example). **All** RF/microwave components have S-parameter files available on the manufacturers' website or can be easily created from traditional datasheets (copy / paste).

Inserting such a model into ADS is made from the "Data Items" palette, where you choose the two-port component (as in the following figure) which allows inserting an external file in various formats, but the data you usually can find is in Touchstone format.




```
!ATF-34143
!S-PARAMETERS at Vds=2V  Id=20mA.  LAST UPDATED 01-29-99
# ghz s ma r 50
! f       S11          S21          S12          S22
! GHz    MAG  ANG     MAG  ANG     MAG  ANG     MAG  ANG
1.0   0.87   -77   8.545   126   0.063   48   0.3   -78
1.5   0.81   -104   7.181   106   0.08   34   0.28   -106
2.0   0.76   -126   6.088   90   0.091   23   0.26   -129
2.5   0.72   -145   5.253   75   0.099   14   0.25   -149
3.0   0.69   -163   4.602   62   0.106   6   0.24   -166
4.0   0.66   166   3.678   38   0.116   -8   0.24   165
5.0   0.65   138   3.058   16   0.124   -22   0.24   138!
!FREQ   Fopt   GAMMA OPT      RN/Zo
!GHZ    dB    MAG    ANG     -
0.5   0.10   0.90   14   0.17
0.9   0.11   0.85   28   0.14
1.0   0.11   0.83   32   0.13
```

Important Note 6. For the project assignment it is recommended to check the presence of the noise parameters in the s2p file at the end (as in the previous figure). Not all bias conditions of a low noise transistor are characterized by good noise performance, and some possible bias points will not have the noise data as their typical usage is in the final stages of an multi-stage amplifier where noise is less important and it is possible that for a low noise transistor there are some s2p files lacking the noise data.

7. Checking transistor's capabilities

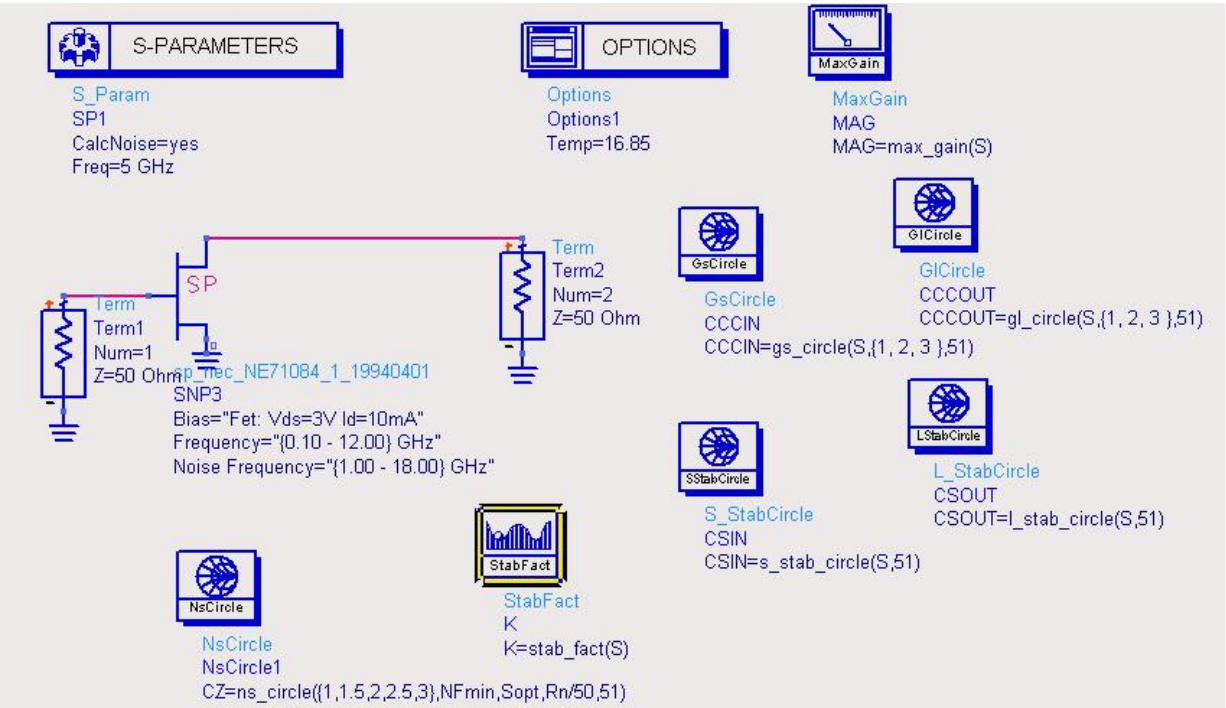
also see Lab3/2021 pts. 4-5

It is recommended that you start with a simple schematic to quickly calculate important parameters for the candidate transistor **at** your specific design frequency. The first and the second schematics from the lab 3 are a good starting point if they can be recovered.

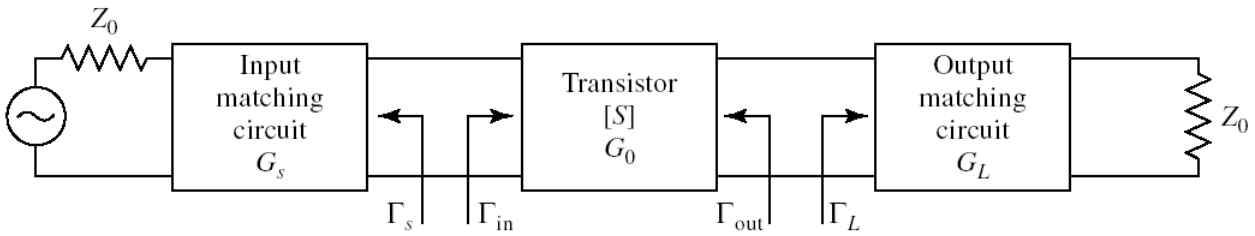
If you cannot manage to compute in ADS the required parameters, or ADS is not available, the calculation of the parameters of interest can be done manually. It is still necessary to represent the stability, gain, noise circles but there are free programs available on the Internet that can do this:

- Avago Appcad (v4.0: https://www.broadcom.com/appcad)
- Smith Chart (v4.10: http://fritz.dellsperger.net/smith.html)

If you use ADS draw a schematic similar to the next figure. The details for drawing the schematic are those from lab 3 and are not repeated here. A common mistake is to perform the analysis with a linear frequency variation, so a minimal check is in the S-Parameters controller, the choice of Single Point analysis, at a frequency equal to the frequency in the individual assignment (5GHz in the sample assignment).



If you don't use ADS to compute the gains available by matching the input/output port of the transistor, then this calculation must be performed manually, those values being necessary to be able to instruct ADS to display the required circles (remember that the circles you request – values between the curly braces {} – depend on the available gains/noise figure for your particular transistor). The modulus of the required S parameters can be very easily read from the S parameter file for 5GHz.

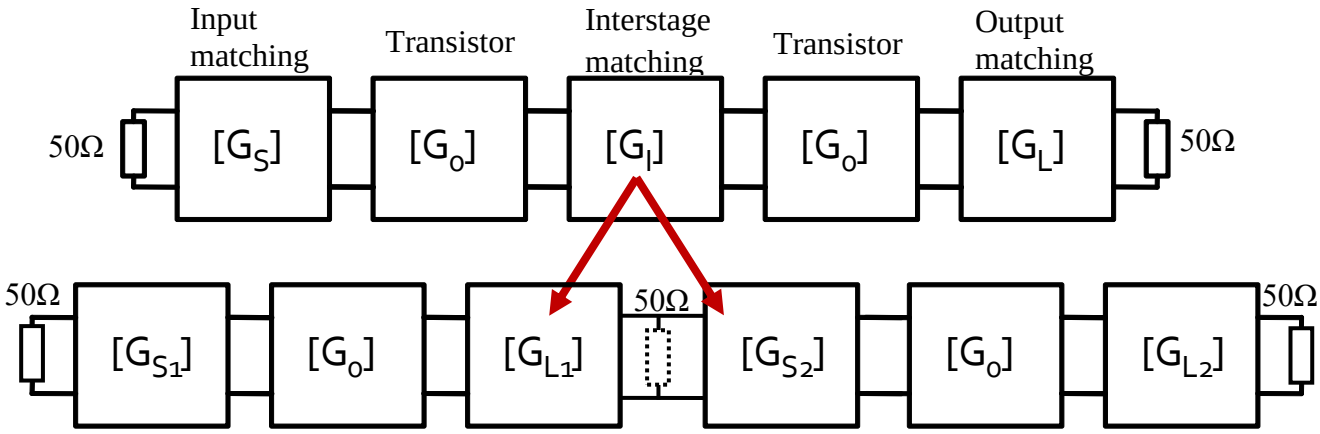


$$G_0 = |S_{21}|^2 = 10.017 = 10.007\ dB$$

$$G_{L\max} = \frac{1}{1-|S_{22}|^2} = 1.051 = 0.215\ dB,\ G_{S\max} = \frac{1}{1-|S_{11}|^2} = 1.694 = 2.289\ dB$$

$$G_{TU\max}[dB] = G_{S\max}[dB] + G_0[dB] + G_{L\max}[dB] = 12.511\,dB$$

In the unilateral transistor assumption, we will obtain a maximum gain of 12.51dB by perfect matching the input and output ports (conditions that probably will not be able to be met). The intrinsic gain of 10.01dB of the transistor will be available, but by input matching we will target a gain of less than 2.29dB (0dB, 1dB, 2dB) and an output gain of less than 0.22dB (-2dB, -1dB , 0dB - remember gains can be negative in dB).



For the design of the matching networks we will use the method of getting a required reflection coefficient (Γ_S, Γ_L) using a series transmission line and a shunt stub, starting from the 50Ω source/load, see L7/2021, S128-140, S165-169.

$$\Gamma = |\Gamma| \cdot e^{j\varphi},\ \cos(\varphi + 2\theta) = -|\Gamma|,\ \theta_{serie} = \beta \cdot l_S = \frac{1}{2} \cdot \left[\pm \cos^{-1}(-|\Gamma|) - \varphi\right] + k \cdot 180°$$

$$\mathrm{Im}[y] = \frac{\mp 2 \cdot |\Gamma|}{\sqrt{1-|\Gamma|^2}},\ \theta_{paralel} = \beta \cdot l_P = \tan^{-1} \frac{\mp 2 \cdot |\Gamma|}{\sqrt{1-|\Gamma|^2}} + k \cdot 180°$$

Important Note 7. Note the possibility/requirement to add 180° multiples to the electrical lengths of the lines to obtain positive values.

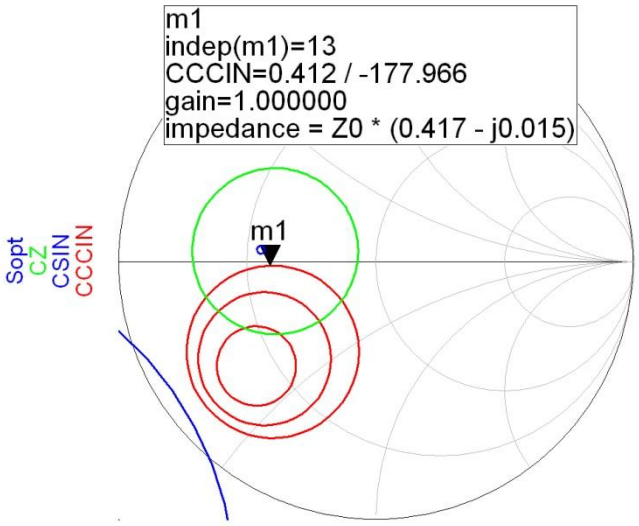
Important Note 8. The equation that provides the electrical length of the series line has two solutions. The sign of the chosen solution imposes the sign used in the shunt stub equation. As a result, there will be (only) **two** solutions for a particular match, both with the similar performance.

For the interstage matching we will use the same method (by matching the two amplification stages to one virtual 50Ω impedance introduced between the two stages: the output match for the first transistor provides one 50Ω impedance and from this 50Ω we design the input match for the second transistor)

8. Design of the input match

The identification of the transmission coefficient needed at the input of the first transistor is done by investigating the circles of stability, gain, noise. As we discussed earlier, in the case of the first amplification stage, it is preferable to favor noise performance by sacrificing (but not too much) the power gain.

The maximum gain that can be obtained by input matching is 2.29dB so we will draw the constant gain circles for 1dB, 1.5dB, 2dB (ie "sacrifice"/loss 1.2dB, 0.7dB, 0.2dB). For this, in ADS it is necessary to modify the equation in the component that draws these circles to CCCIN=gs_circle(S,{1,1.5,2},100) where 100 (or other value) is the number of points on the circle circumference calculated (more will give a better accuracy in positioning the marker on these circles). Draw the noise circle for 0.75dB (close to the 0.7dB required) and the minimum noise point (optimal reflection coefficient for minimum noise figure). The input stability circle **must** also be represented (the noise/gain of the device does not matter if the device is unstable).



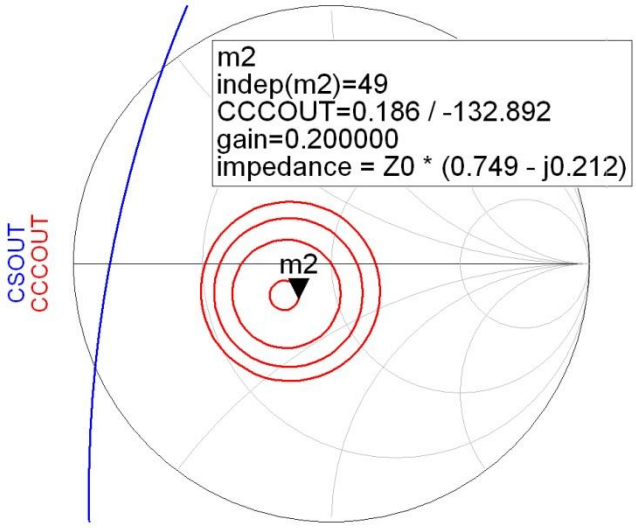
A convenient position is the one indicated with the m1 marker, positioning the marker on the 1dB gain circle meaning decreasing with 1.2dB the achievable gain, but this position is well inside the 0.75dB noise circle (actually close to the minimum noise point, so we can expect a noise factor close to the minimum of 0.54dB) and away from the circle stability. In this position we can read in ADS from the marker legend the value of the reflection coefficient we need to obtain (0.412∠-178°). If you use other software the display might be different (usually the instantaneous position of the cursor is displayed somewhere).

$$\cos(\varphi_{S1}+2\theta)=-|\Gamma_{S1}|,\ \mathrm{Im}[y_{S1}(\theta)]=\frac{\mp 2\cdot|\Gamma_{S1}|}{\sqrt{1-|\Gamma_{S1}|^2}}$$

Equation	Solution S1A	Solution S1B
$(\varphi_{S1}+2\theta)$	+114.33°	−114.33°
$\theta_{serie}=\frac{1}{2}\cdot\left[\pm\cos^{-1}(-\lvert\Gamma_{S1}\rvert)-\varphi_{S1}\right]+k\cdot 180°$	**146.2°**	31.8°
$\mathrm{Im}[y_{S1}(\theta)]=\frac{\mp 2\cdot\lvert\Gamma_{S1}\rvert}{\sqrt{1-\lvert\Gamma_{S1}\rvert^2}}$	−0.904	+0.904
$\theta_{paralel}=\tan^{-1}\frac{\mp 2\cdot\lvert\Gamma_{S1}\rvert}{\sqrt{1-\lvert\Gamma_{S1}\rvert^2}}+k\cdot 180°$	**137.9°**	42.1°

9. Design of the output match

The identification of the transmission coefficient needed at the output of the second transistor is done by investigating the stability and gain circles (the noise introduced by the second transistor is not influenced in any way by its output match). Because noise is not an issue, output match can aim to optimize gain. The maximum gain that can be obtained by output matching is 0.22dB so we will draw the constant gain circles for 0.2dB, 0dB, -0.2dB, -0.4dB (ie "sacrifice"/loss of 0.02dB, 0.22dB, 0.42dB, 0.62dB). For this, in ADS it is necessary to modify the equation in the component that draws these circles CCCOUT=gl_circle(S,{-0.4,-0.2,0,0.2},100).



A convenient position is the one indicated with the m2 marker, positioning the marker on the 0.2dB gain circle meaning a gain close to the maximum, far from the stability circle (there is no need to sacrifice gain to improve stability). Note that the 0dB gain circle passes through the center of the Smith Chart (**always**) so an honorable behavior (0.22dB gain loss) can be obtained without output matching (direct connection of the transistor to 50Ω - solution that is not generally recommended, the flexibility of the schematic is lost, we eliminate two lines which can be adjusted to correct certain

deficiencies). In the m2 position we can read in ADS marker legend the value of the reflection coefficient we need (0.186∠-132.9°).

$$\cos(\varphi_{L2}+2\theta)=-|\Gamma_{L2}|, \qquad \mathrm{Im}[y_{L2}(\theta)]=\frac{\mp 2\cdot|\Gamma_{L2}|}{\sqrt{1-|\Gamma_{L2}|^2}}$$

Equation	Solution L2A	Solution L2B
$(\varphi_{L2}+2\theta)$	+100.72°	−100.72°
$\theta_{serie}=\frac{1}{2}\cdot\left[\pm\cos^{-1}(-\lvert\Gamma_{L2}\rvert)-\varphi_{L2}\right]+k\cdot 180°$	**116.8°**	16.1°
$\mathrm{Im}[y_{L2}(\theta)]=\frac{\mp 2\cdot\lvert\Gamma_{L2}\rvert}{\sqrt{1-\lvert\Gamma_{L2}\rvert^2}}$	−0.379	+0.379
$\theta_{paralel}=\tan^{-1}\frac{\mp 2\cdot\lvert\Gamma_{L2}\rvert}{\sqrt{1-\lvert\Gamma_{L2}\rvert^2}}+k\cdot 180°$	**159.3°**	20.7°

10. Design of the interstage match

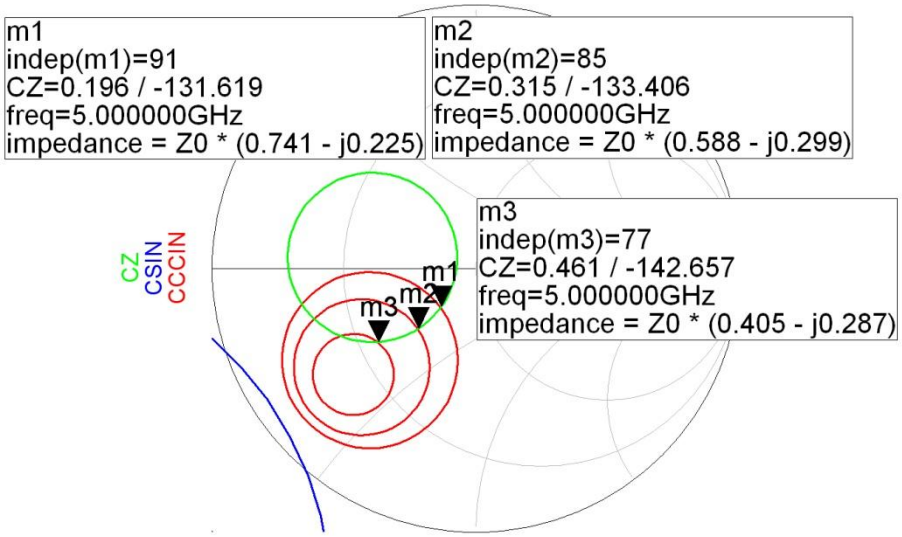
As mentioned earlier, the interstage match between the output of the first transistor and the input of the second transistor consists of a combination of two matches to a virtual impedance of 50Ω.

The output of the first transistor will be matched to this virtual impedance. Because we used the same transistor, and because the considerations are the same (the noise introduced by the first transistor is not influenced in any way by its output match) the line/stub performing the match may be identical to those previously chosen (Γ = 0.186∠-132.9°).

$$\cos(\varphi_{L1}+2\theta)=-|\Gamma_{L1}|\,,\ \mathrm{Im}[y_{L1}(\theta)]=\frac{\mp 2\cdot|\Gamma_{L1}|}{\sqrt{1-|\Gamma_{L1}|^2}}$$

Equation	Solution L1A	Solution L1B
$(\varphi_{L1}+2\theta)$	+100.72°	−100.72°
$\theta_{serie}=\frac{1}{2}\cdot\left[\pm\cos^{-1}(-\lvert\Gamma_{L1}\rvert)-\varphi_{L1}\right]+k\cdot 180°$	116.8°	16.1°
$\mathrm{Im}[y_{L1}(\theta)]=\frac{\mp 2\cdot\lvert\Gamma_{L1}\rvert}{\sqrt{1-\lvert\Gamma_{L1}\rvert^2}}$	−0.379	+0.379

For the match of the input of the second transistor to the virtual 50Ω impedance, we will have a similar situation with the input match of the first transistor, but this time the noise is not as important (Friis formula shows that a noise factor of even of 1dB is acceptable), so we will have greater flexibility in choosing the point (reflection coefficient at the input of the second transistor).



We will be able to choose the position indicated by the marker m3 (0.461∠-142.66°) for which we obtain the solution listed below. If we later encounter stability problems we can try to improve it by choosing another point (for example m1, farther from the stability circle but a gain reduced by 1dB).

$$\cos(\varphi_{S2}+2\theta)=-|\Gamma_{S2}|, \qquad \mathrm{Im}[y_{S2}(\theta)]=\frac{\mp 2\cdot|\Gamma_{S2}|}{\sqrt{1-|\Gamma_{S2}|^2}}$$

Equation	Solution S2A	Solution S2B
$(\varphi_{S2}+2\theta)$	+117.45°	−117.45°
$\theta_{serie}=\frac{1}{2}\cdot\left[\pm\cos^{-1}(-\lvert\Gamma_{S2}\rvert)-\varphi_{S2}\right]+k\cdot 180°$	130.1°	12.6°
$\mathrm{Im}[y_{S2}(\theta)]=\frac{\mp 2\cdot\lvert\Gamma_{S2}\rvert}{\sqrt{1-\lvert\Gamma_{S2}\rvert^2}}$	−1.039	+1.039

We designed the two matching networks to the virtual 50Ω impedance, next we must combine them into a single interstage network, see L10/2021, S 68-97. In the case of two previous networks, the electrical length of each shunt stub was not calculated because it is not needed. The two stubs will be positioned (both) at the level of the virtual 50Ω impedance. As a result, their admittances will add (being in parallel) and we can use a single stub instead of two to implement the resulting admittance.

$$\mathrm{Im}[y_{L1}(\theta_{L1})]=\frac{\mp 2\cdot|\Gamma_{L1}|}{\sqrt{1-|\Gamma_{L1}|^2}} \qquad \mathrm{Im}[y_{S2}(\theta_{S2})]=\frac{\mp 2\cdot|\Gamma_{S2}|}{\sqrt{1-|\Gamma_{S2}|^2}}$$

$$\mathrm{Im}[y_{50\Omega}]=\mathrm{Im}[y_{L1}(\theta_{L1})]+\mathrm{Im}[y_{S2}(\theta_{S2})]=\frac{\pm 2\cdot|\Gamma_{L1}|}{\sqrt{1-|\Gamma_{L1}|^2}}+\frac{\pm 2\cdot|\Gamma_{S2}|}{\sqrt{1-|\Gamma_{S2}|^2}},$$

$$\theta_{shunt}=\tan^{-1}\mathrm{Im}[y_{50\Omega}]+k\cdot 180°$$

Because for each of the two admittances we have two distinct solutions (+/−) there will be 4 distinct possibilities to combine the two matching networks.

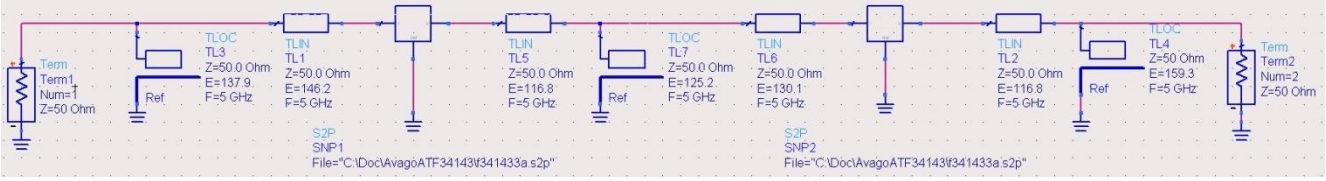
		Solution S2A	Solution S2B
		$\mathrm{Im}[y_{S2}(\theta)] = -1.039$ $\theta_{S2} = 130.1°$	$\mathrm{Im}[y_{S2}(\theta)] = +1.039$ $\theta_{S2} = 12.6°$
Solution L1A	$\mathrm{Im}[y_{L1}(\theta)] = -0.379$ $\theta_{L1} = 116.8°$	$\theta_{L1} = 116.8°$ $\mathrm{Im}[y_{50\Omega}] = -1.418$ $\theta_{shunt} = 125.2°$ $\theta_{S2} = 130.1°$	$\theta_{L1} = 116.8°$ $\mathrm{Im}[y_{50\Omega}] = +0.66$ $\theta_{shunt} = 33.4°$ $\theta_{S2} = 12.6°$
Solution L1B	$\mathrm{Im}[y_{L1}(\theta)] = +0.379$ $\theta_{L1} = 16.1°$	$\theta_{L1} = 16.1°$ $\mathrm{Im}[y_{50\Omega}] = -0.66$ $\theta_{shunt} = 146.6°$ $\theta_{S2} = 130.1°$	$\theta_{L1} = 16.1°$ $\mathrm{Im}[y_{50\Omega}] = +1.418$ $\theta_{shunt} = 54.8°$ $\theta_{S2} = 12.6°$

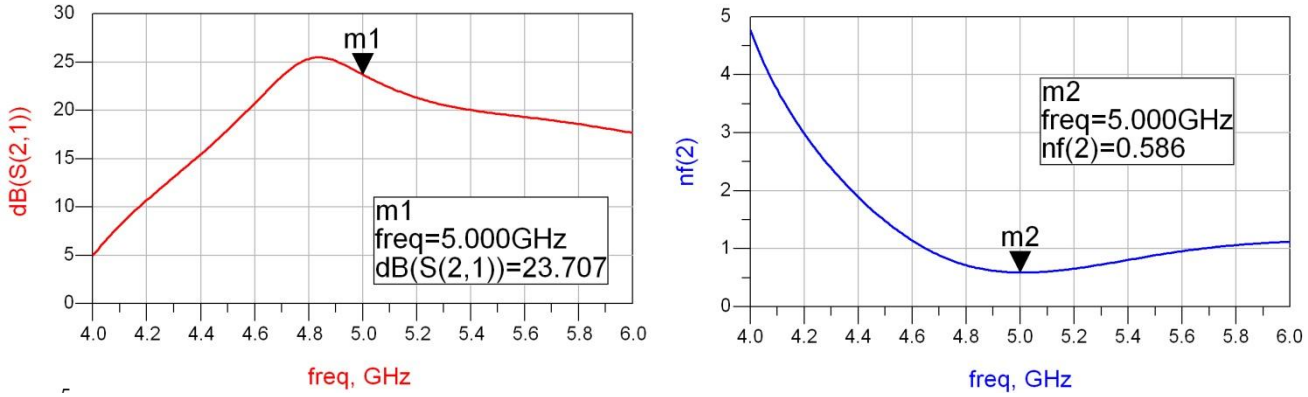
11. Draw and simulate the complete amplifier

For the implementation of the amplifier, one of the possible solutions must be chosen for each matching network. In principle, too short lines will be difficult to implement and will physically bring various devices/stubs nearby leading to unwanted coupling so they should be avoided, while too long lines will take up too much (unnecessary) space on the circuit board. All characteristic impedances are equal to $Z_0 = 50\Omega$

- for input matching we choose solution S1A, order from input to output:
  - shunt stub with E = 137.9°
  - series line with E = 146.2°
- for interstage matching we choose solution L1A/S2A, order from input to output:
  - series line with E = 116.8°
  - shunt stub with E = 125.2°
  - series line with E = 130.1°
- for output matching we choose solution L2A, order from input to output:
  - series line with E = 116.8°
  - shunt stub with E = 159.3°

We can draw the complete schematic and verify if computations for the matching networks were correct (we obtain the expected gain/noise factor). As instructed in the lab, it is possible to draw the schematics/simulate the two stages individually to verify them in turn, but at this point we can verify the entire amplifier.



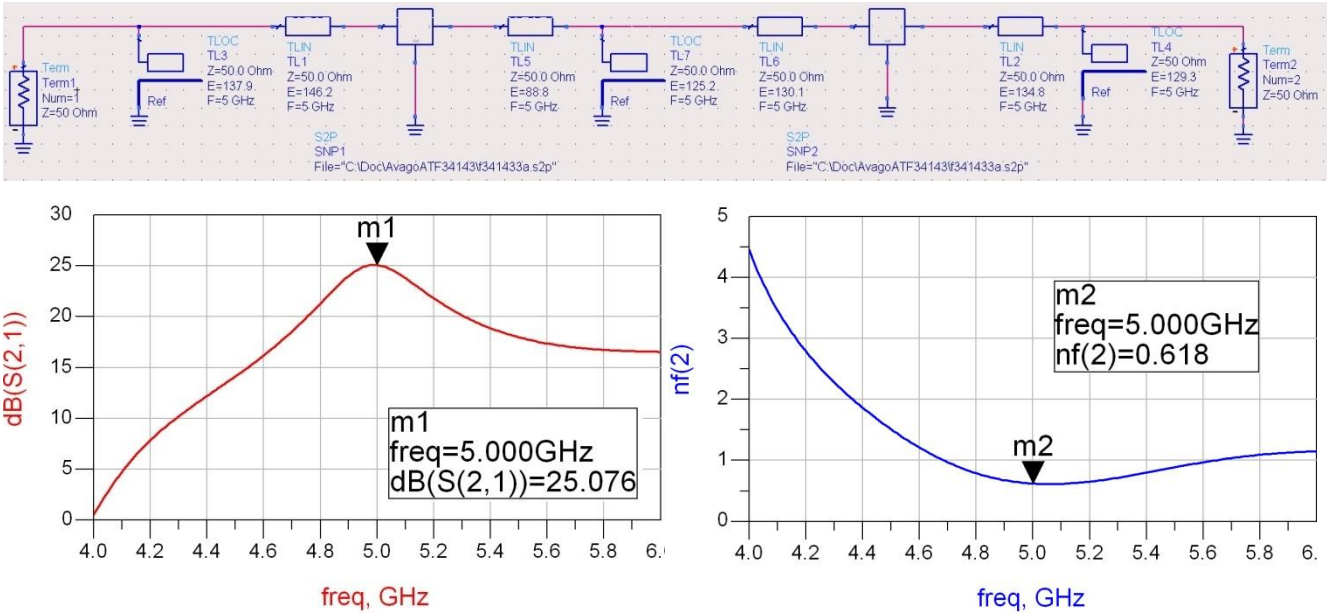


12. Balance the amplifier gain

The gain and noise results meet the requirements of the sample assignment with a sufficient reserve for the gain and a noise factor very close to the minimum (much smaller, so better than a noise factor F = 0.85dB initially estimated). The only problem is that the amplifier does not have the maximum gain at 5GHz, which will unbalance the final result.

We want to move the peak of the gain to 5GHz, if possible without affecting the gain and noise factor. It is preferable to adjust the components (electrical lengths of the lines) starting from the output to the input because in this way the noise factor is not at all influenced (output matching network) or is less influenced (interstage matching network). If this is not possible without the excessive impact over the power gain only then, **as a last resort**, the two input lines can also be adjusted.

Following the adjustment, balancing can be achieved in the sample assignment by adjusting the lengths of the output lines and one of the lines in the interstage network, with only minor effect (slight increase) on the noise factor.



13. Design of the passband filter

also see L9/2021, S 138-147

The first step in filter design is to choose the technology. In order to maintain the advantage of using lines instead of lumped elements (2p) it is preferred to use a filter implemented with transmission lines. We will design a coupled line filter. However, remember that there is a bonus for using a different filter type, so you could investigate filters with capacitively coupled series resonators or with lines as resonators.

For the bandpass filter with coupled lines we have the design relations:

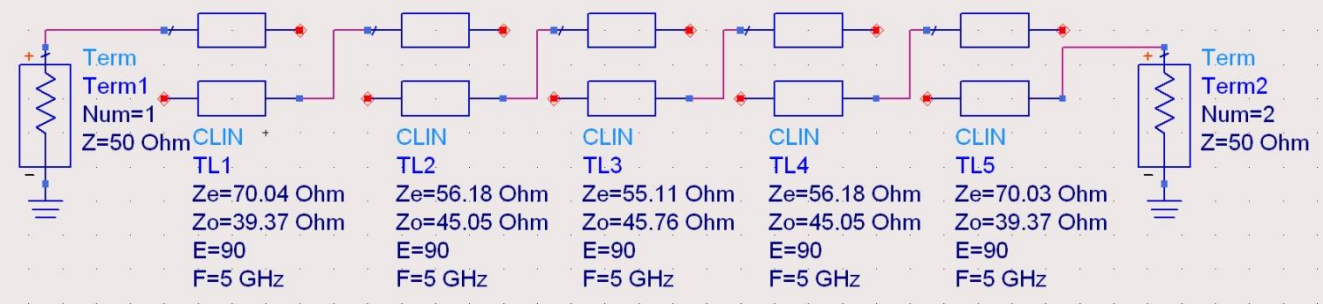
$$Z_0 \cdot J_1 = \sqrt{\frac{\pi \cdot \Delta}{2 \cdot g_1}} \qquad Z_0 \cdot J_n = \frac{\pi \cdot \Delta}{2 \cdot \sqrt{g_{n-1} \cdot g_n}}, n = \overline{2, N} \qquad Z_0 \cdot J_{N+1} = \sqrt{\frac{\pi \cdot \Delta}{2 \cdot g_N \cdot g_{N+1}}}$$

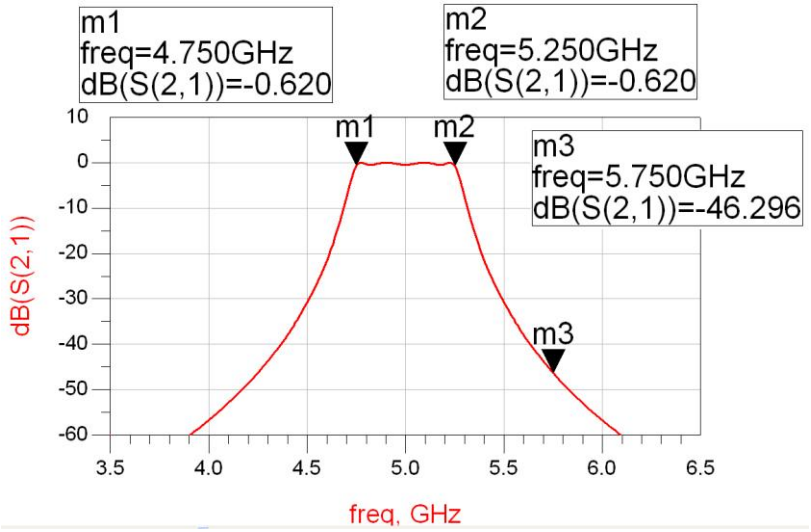
$$Z_{0o,n} = Z_0 \cdot \left[1 - J_n \cdot Z_0 + (J_n \cdot Z_0)^2\right] \qquad Z_{0e,n} = Z_0 \cdot \left[1 + J_n \cdot Z_0 + (J_n \cdot Z_0)^2\right] \qquad n = \overline{1, N+1}$$

We choose a 4th order equal-ripple filter, with 0.5dB ripple, coefficients from the corresponding table. The bandpass 4th order filter with coupled lines will be implemented with 5 sections of coupled lines (bandwidth 10%, Δ=0.1).

n	**g_n**	**Z_0J_n**	**Z_{0e} [Ω]**	**Z_{0o} [Ω]**
1	1.6703	0.306664	70.04	39.37
2	1.1926	0.111295	56.18	45.05
3	2.3661	0.09351	55.11	45.76
4	0.8419	0.111294	56.18	45.05
5	1.9841	0.306653	70.03	39.37

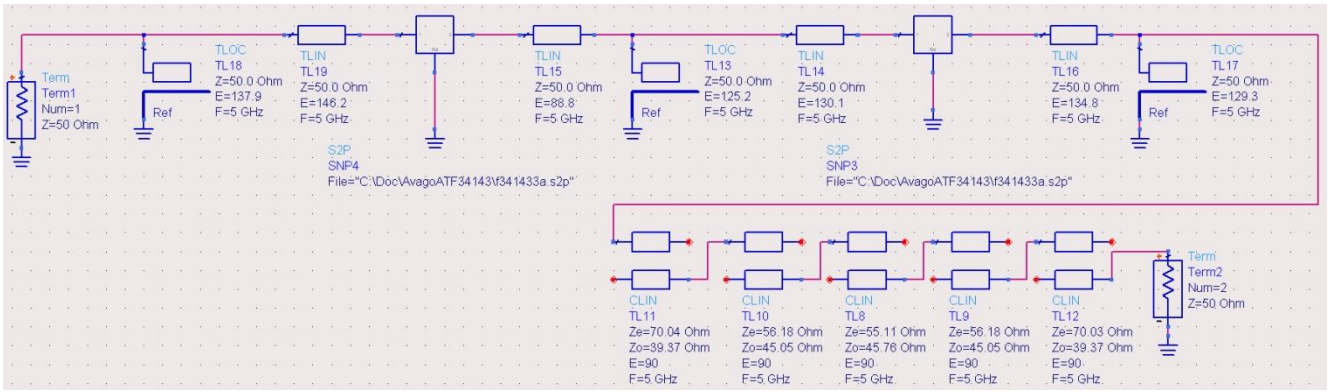
We can verify the filter in a separate schematic.

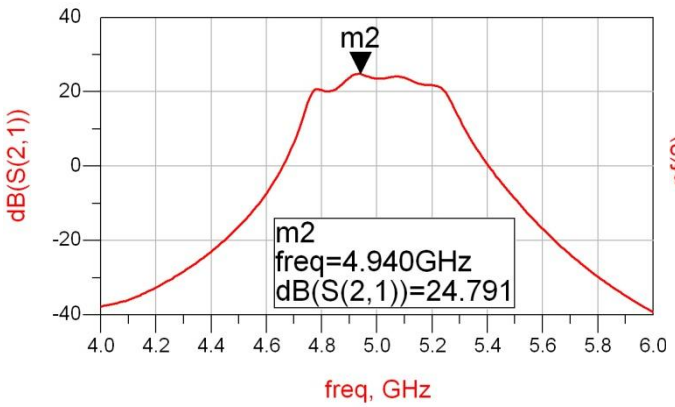


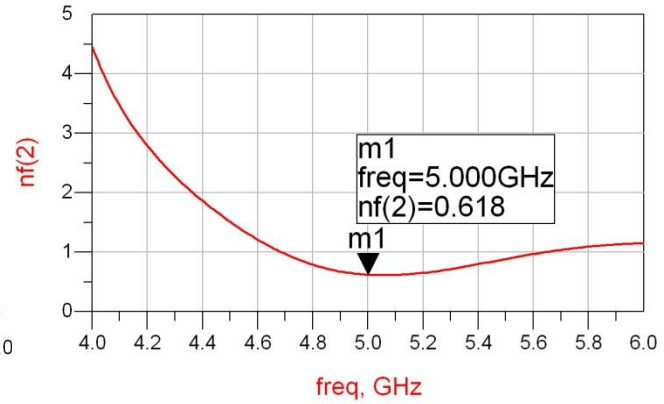


14. Final schematic

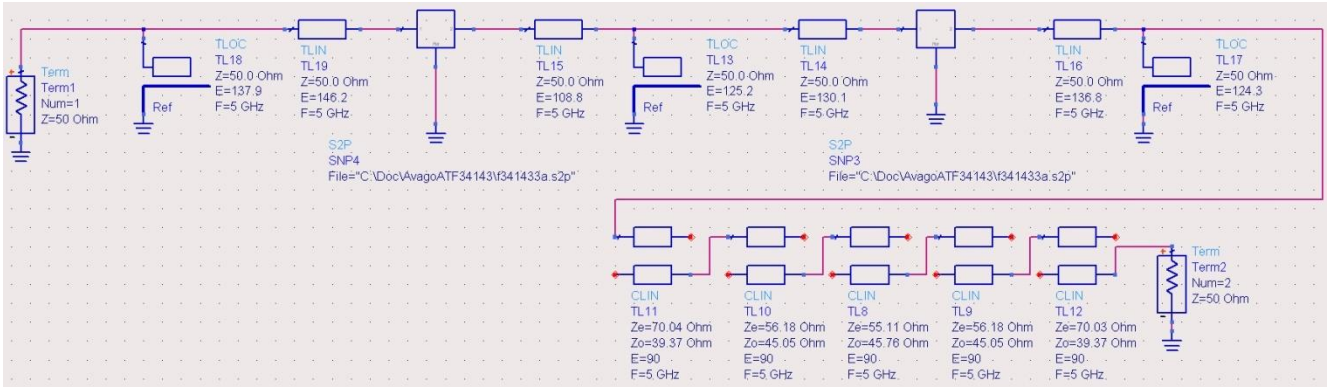
For the final schematic, the amplifier and the filter are connected together. The filter can be connected before or after the amplifier.

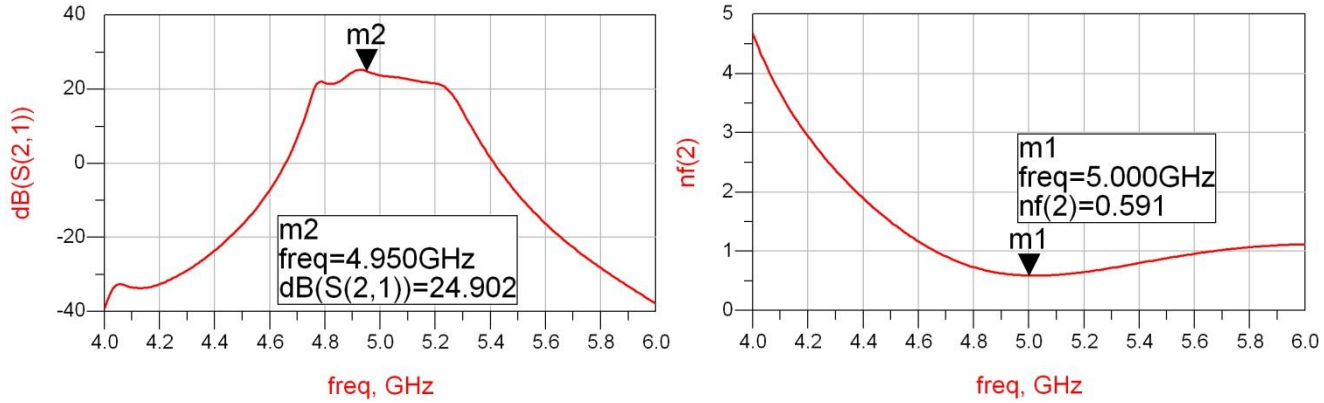






The only problem with the final schematic is that at low frequencies at the end of the passband (~4.75GHz) we have a decrease of the gain. This can be compensated by a final adjustment of the transmission lines, preferably with the adjustment of the line in the interstage matching network, whose adjustment altered the noise factor.





After the final tune, a slightly better noise factor is obtained (F = 0.591dB) and a power gain with a ripple of approximately 3dB in the bandwidth, between 4.75GHz and 5.25GHz, with a minimum of 21.6dB and a maximum of 24.9dB.

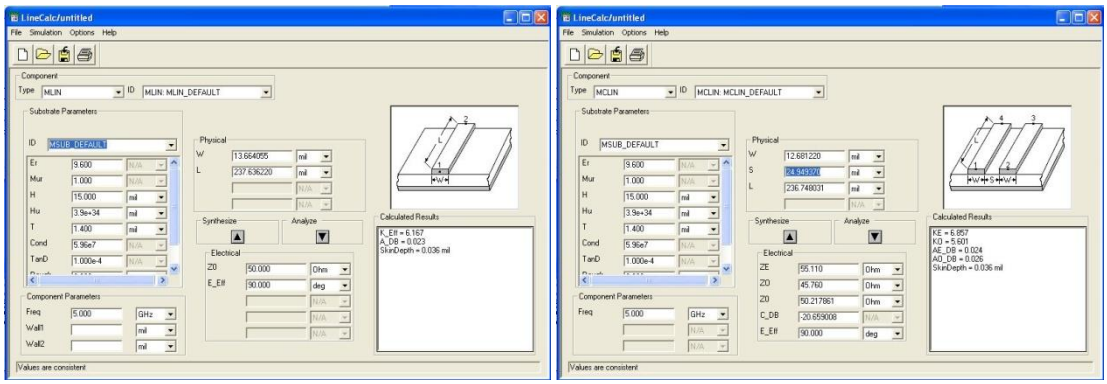
The above schematic corresponds to project assignment graded with 10 (if transistors other than those prohibited/penalized are used). The final remark is that in real situations the discussion would not be complete without the analysis of stability and possibly forcing the stability of the circuit (see L8/2021, S 101-115)

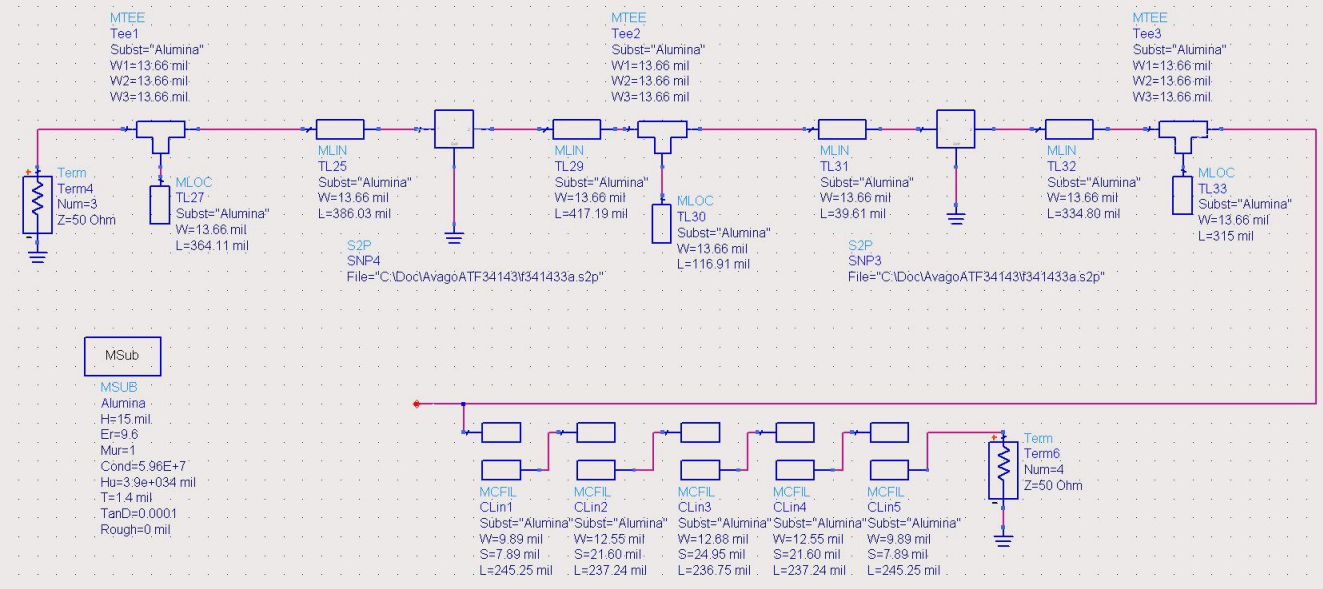
15. Additional points

One additional point can be obtained if two different transistors are used for the two amplification stages (chosen accordingly: low noise for the first stage, high gain for the second stage).

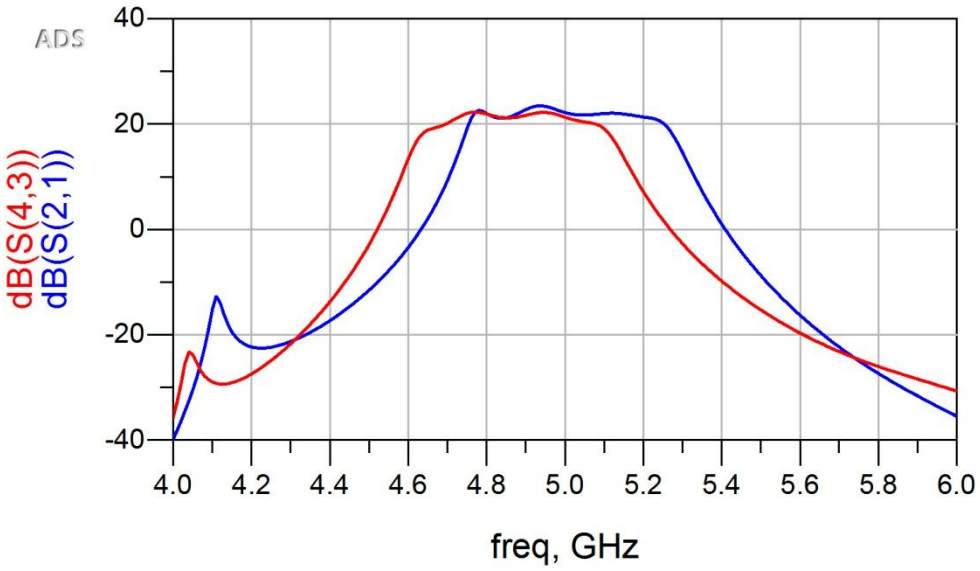
Another additional point can be obtained if you use a different type for the filter than coupled lines filter.

The implementation of the lines in microstrip technology, microstrip line models **and** the modeling of transition blocks between various lines (MTEE, MSTEP) can bring up to two extra points. You will have to use the ADS tool Linecalc or an online equivalent.

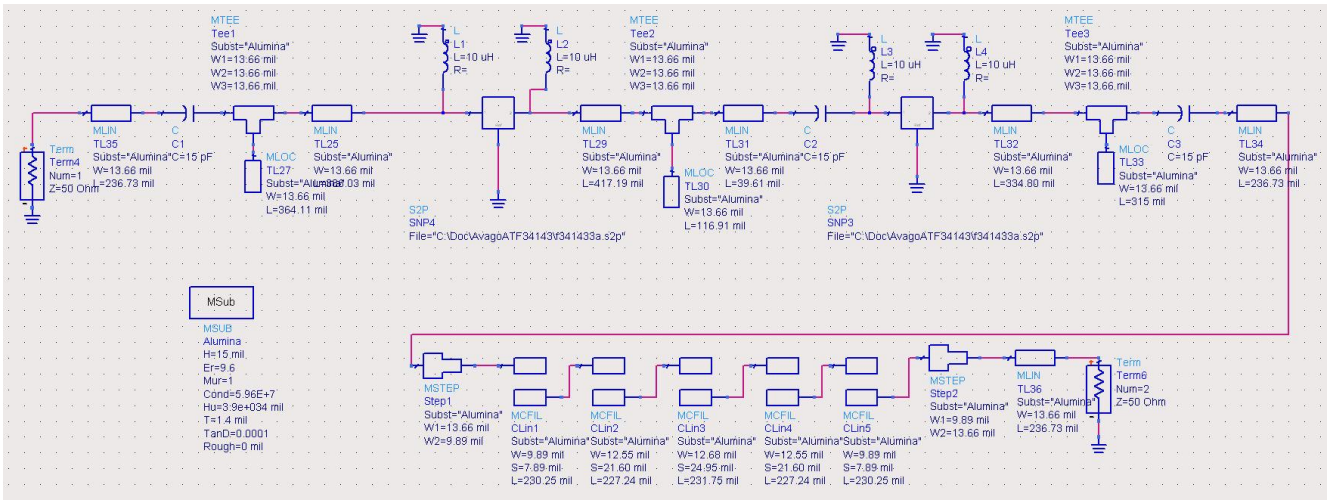


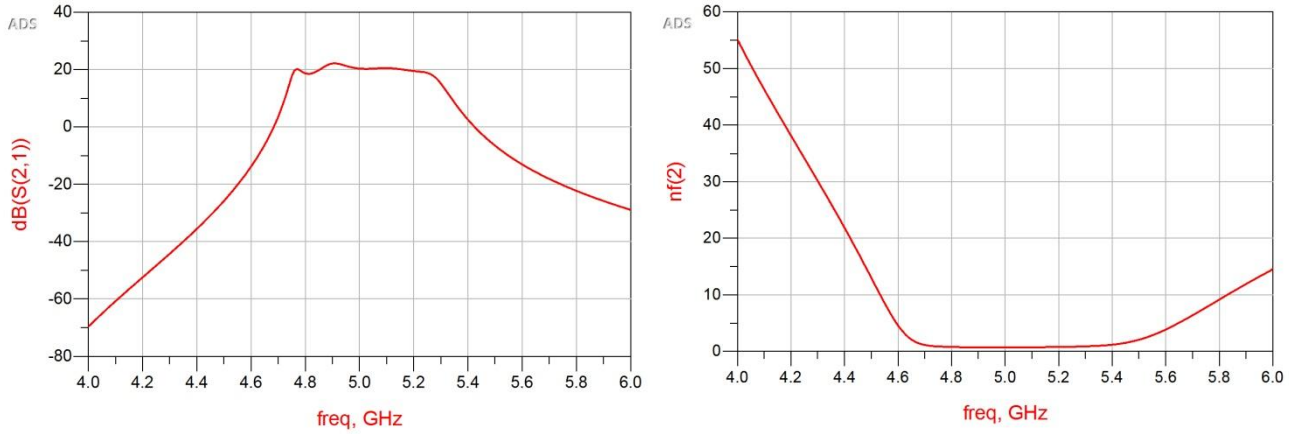


Instead of the coupled line microstrip model (MCLIN), you should use the coupled line filter section model (MCFIL), a more accurate model than MCLIN because it takes into account that two successive sections are physically joined. Investigating the results, there is a shift of the transfer function (red) towards lower frequencies than the ideal models (blue) due to the MCFIL/MCLIN difference. The correction of this shift is done by a slight adjustment (Tune) of the length of the coupled line sections.

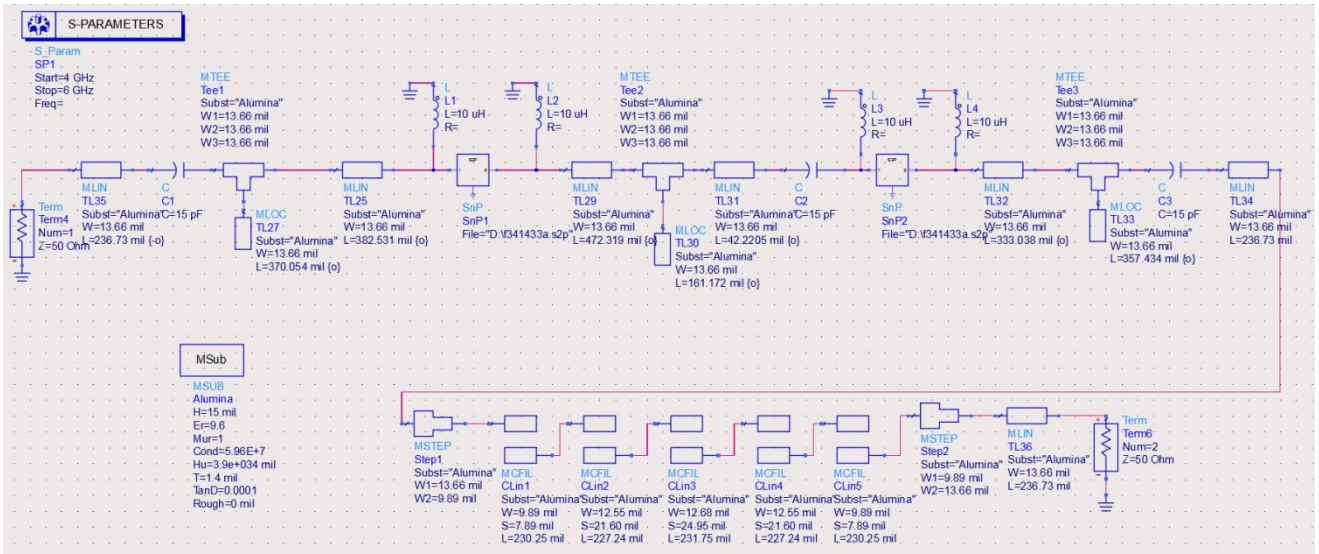


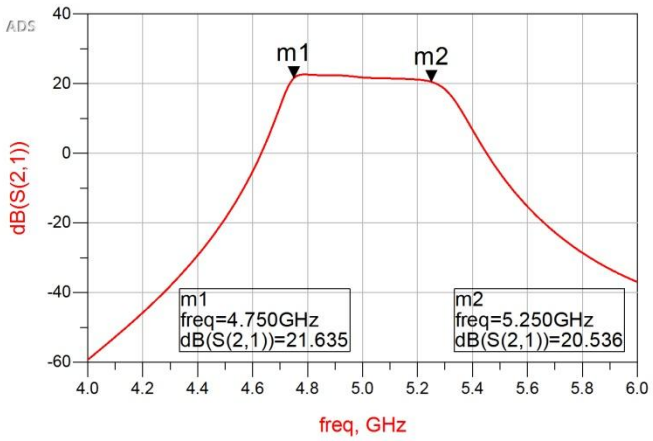
Designing the complete biasing schematic (direct current) for both transistors (source voltage, decoupling capacitors, RF chokes) can bring you one extra point. The introduction of the bias components into the final schematic (with their parasitic elements and with additional 50Ω connection lines and the modeling of possible transitions between the lines) can bring an additional point.

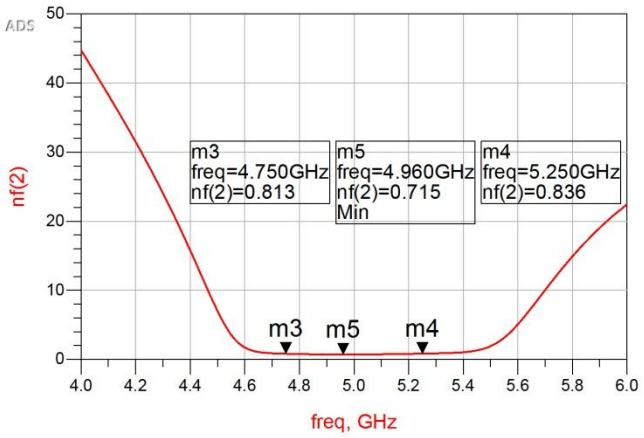




For the sample assignment inserting the biasing components in the schematic decreases the gain below the minimum gain condition of 20dB in a restricted frequency range. A final adjustment/ optimization of the schematic provides the fulfillment of this criterion.







The complete additional score (2p) for the bias schematic is obtained for the use of the complete low level schematic for the transistor and the complete DC/AC simulation circuit (including resistive dividers, filtering capacitors, etc.) and might not be available for all transistors (you are restricted to the transistors types for which you can find the complete ADS model).