Laboratory 5 (w11-14)

2023/2024

Microwave Devices and Circuits for Radiocommunications

MDCR Project

Assignment

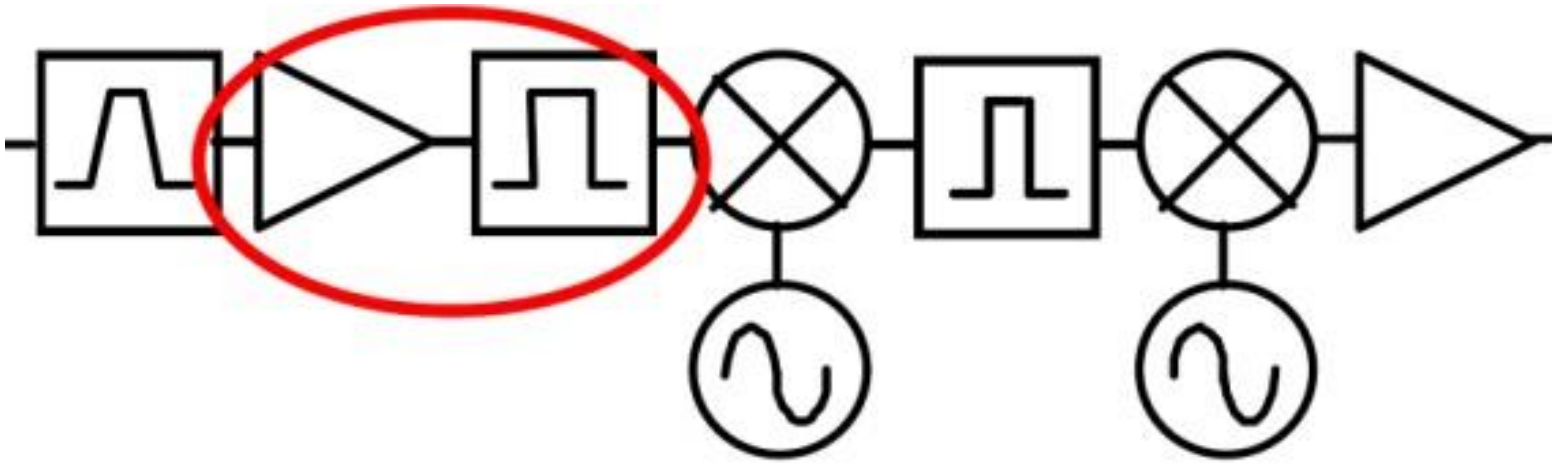
- Design a low-noise multi-stage transistor amplifier required to provide a power gain of **G [dB]** and a noise factor of **F [dB]** at the design frequency **f [GHz]**.
- At the output of the amplifier insert a order **N** bandpass filter with fractional bandwidth of the passband **B [%]** around the design frequency.

Assignment

- The matching networks and filter must be implemented with transmission lines (stubs: L7-L8).
- The use of the transistors we used in lectures and laboratories examples is not permitted (NE 71084, ATF 34143)
- Delivery deadline: last day of the semester (06.06.2021, 23:59:59)

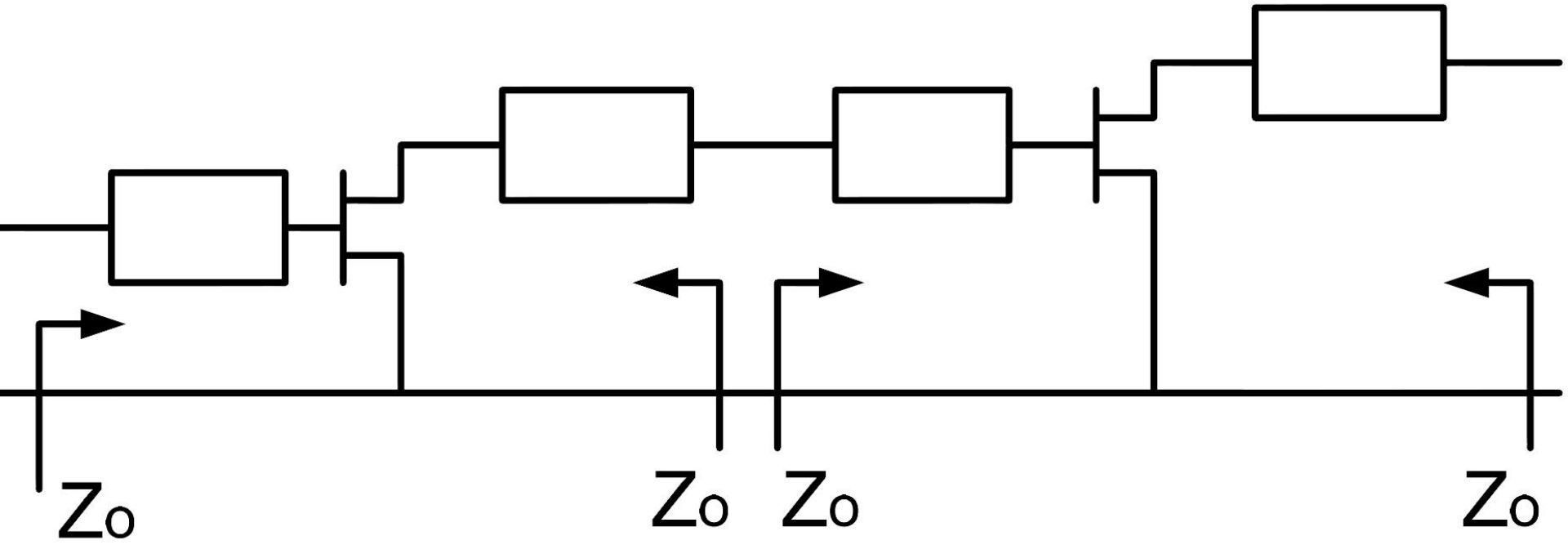
Assignment

- this structure is frequently encountered in radiocommunication systems

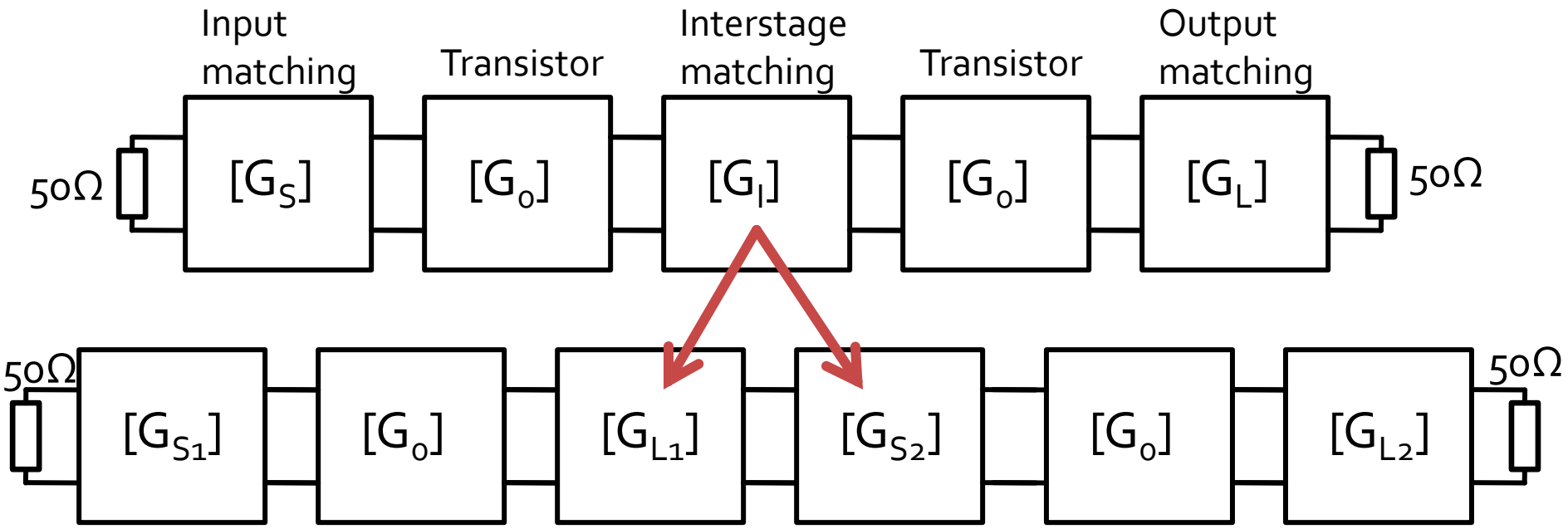


Multistage amplifiers

- Interstage matching can be designed in two modes:
  - Each stage is matched to a virtual Γ = 0



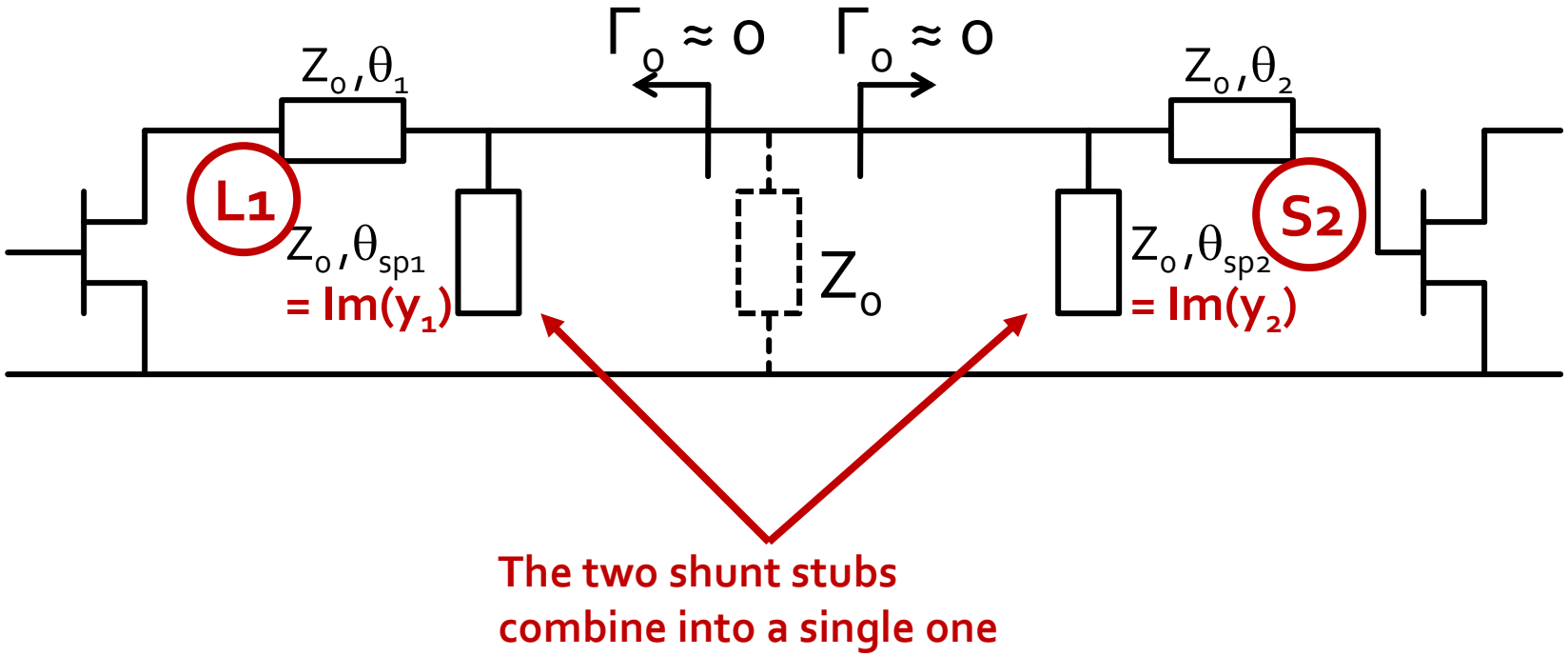
Multistage amplifier design



- The design for input and output matching must be achieved on a single transistor schematic (recommended: easier)

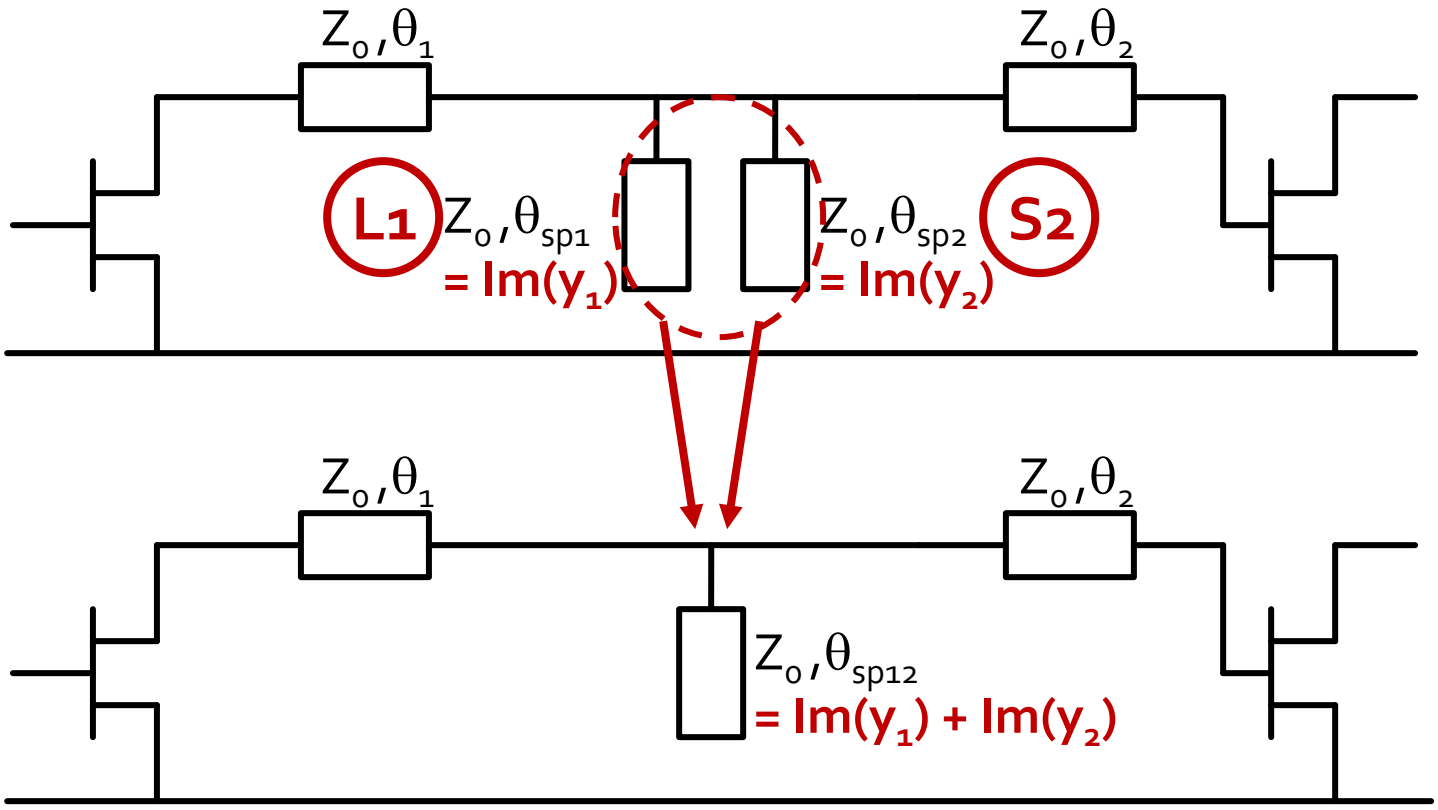
Interstage matching

- One of the stages creates through its matching network a refflection coefficient Γ=0 towards which the other stage is matched



Interstage matching

- The two shunt stubs combine into a single one



Practical Procedure

Step - 1

- Split performance parameters on the 2 stages
  - G
  - F
- Uses Friis formula
- Pt. 3 example

$$G_{cas} = G_1 \cdot G_2 \qquad F_{cas} = F_1 + \frac{1}{G_1}(F_2 - 1)$$

- 2 equations, 4 unknowns, multiple solutions

Friis Formula (noise)

$$G_{cas} = G_1 \cdot G_2 \qquad F_{cas} = F_1 + \frac{1}{G_1}(F_2 - 1)$$

- Friis formula
  - first stage: low noise factor, probably resulting in a smaller gain
  - second stage: high gain, probably resulting in higher noise factor
- It's essential to introduce a design margin (reserve: ΔF, ΔG)
  - $G = G_{design} + \Delta G$
  - $F = F_{design} - \Delta F$
- Interpretation of the design target
  - $G > G_{design}$, better, but it's not required to sacrifice other parameters to maximize the gain
  - $F < F_{design}$, better, the smaller the better, we must target **the smallest possible noise** factor as long as the other design parameters **are met**

Friis Formula (noise)

- Friis formula
  - first stage: low noise factor, probably resulting in a smaller gain
  - second stage: high gain, probably resulting in higher noise factor
- Division between the two stages (Estimated!)
  - input stage: F1 = 0.7 dB, G1 = 9 dB
  - output stage: F2 = 1.2 dB, G2 = 13 dB
- To verify the result apply Friis formula
- First transform to **linear scale !**

$$F_1 = 10^{\frac{F_1[dB]}{10}} = 10^{0.07} = 1.175 \qquad G_1 = 10^{\frac{G_1[dB]}{10}} = 10^{0.9} = 7.943$$

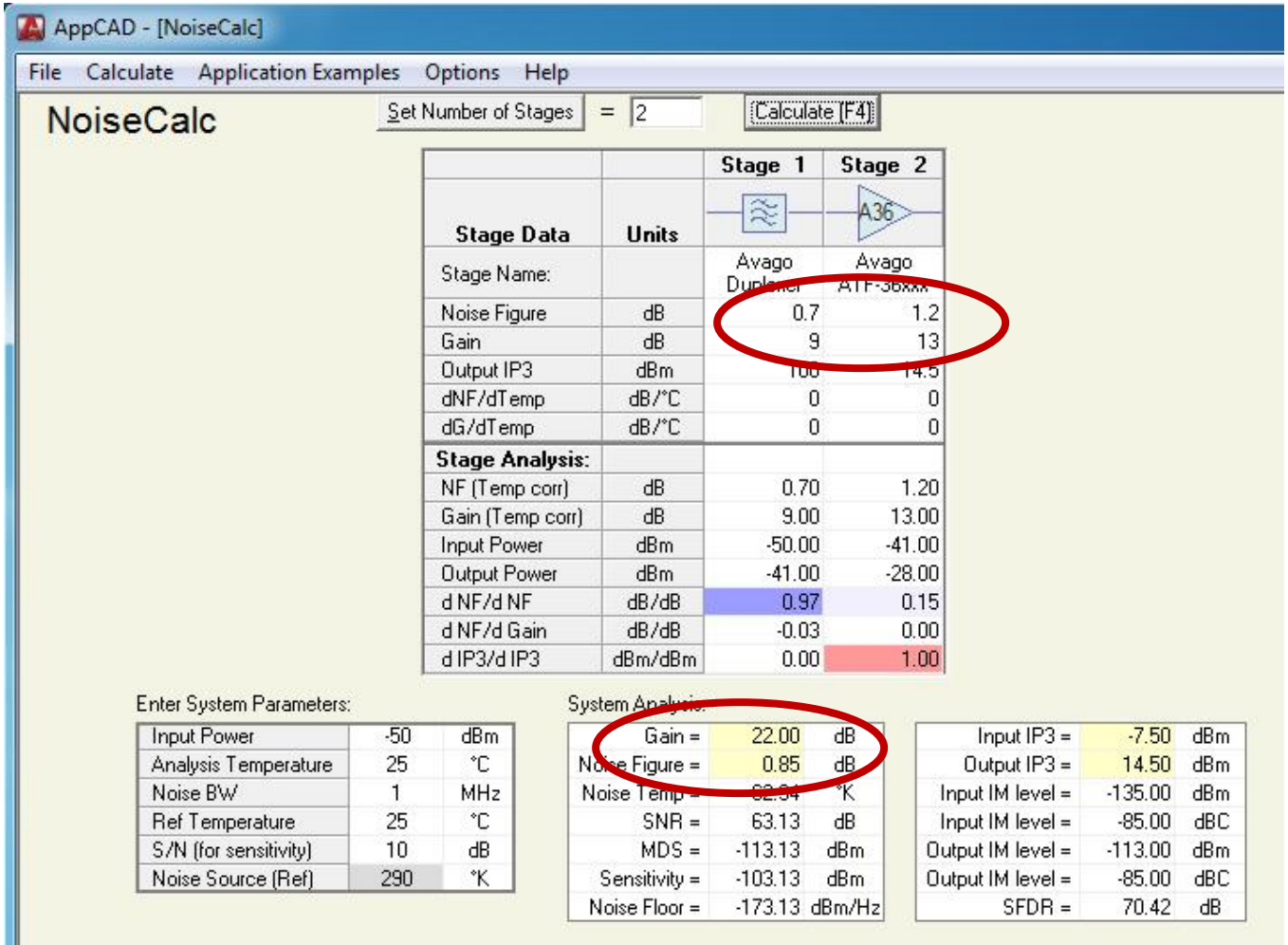
$$F_2 = 10^{\frac{F_2[dB]}{10}} = 10^{0.12} = 1.318 \qquad G_2 = 10^{\frac{G_2[dB]}{10}} = 10^{1.3} = 19.953$$

$$F_{cas} = F_1 + \frac{1}{G_1}(F_2 - 1) = 1.215 \qquad G_{cas} = G_1 \cdot G_2 = 158.49$$

$$F_{cas} = 10 \cdot \log(1.215) = 0.846\,dB \qquad G_{cas} = 10 \cdot \log(158.49) = 22\,dB$$

Friis Formula (noise)

- Avago/Broadcom AppCAD



AppCAD - [NoiseCalc]

File Calculate Application Examples Options Help

NoiseCalc

Set Number of Stages = 2 Calculate [F4]

Stage Data	Units	Stage 1	Stage 2
Stage Name:		Avago Duplexer	Avago ATF-36xxx
Noise Figure	dB	0.7	1.2
Gain	dB	9	13
Output IP3	dBm	100	14.5
dNF/dTemp	dB/°C	0	0
dG/dTemp	dB/°C	0	0
Stage Analysis:			
NF (Temp corr)	dB	0.70	1.20
Gain (Temp corr)	dB	9.00	13.00
Input Power	dBm	-50.00	-41.00
Output Power	dBm	-41.00	-28.00
d NF/d NF	dB/dB	0.97	0.15
d NF/d Gain	dB/dB	-0.03	0.00
d IP3/d IP3	dBm/dBm	0.00	1.00

Enter System Parameters:

Input Power	-50	dBm
Analysis Temperature	25	°C
Noise BW	1	MHz
Ref Temperature	25	°C
S/N (for sensitivity)	10	dB
Noise Source (Ref)	290	°K

System Analysis:

Gain =	22.00	dB
Noise Figure =	0.85	dB
Noise Temp =	62.94	°K
SNR =	63.13	dB
MDS =	-113.13	dBm
Sensitivity =	-103.13	dBm
Noise Floor =	-173.13	dBm/Hz

Input IP3 =	-7.50	dBm
Output IP3 =	14.50	dBm
Input IM level =	-135.00	dBm
Input IM level =	-85.00	dBC
Output IM level =	-113.00	dBm
Output IM level =	-85.00	dBC
SFDR =	70.42	dB

Step - 1

- Result:
  - first amplifier **G1/F1**
  - second amplifier **G2/F2**

Step - 2

- Choose appropriate transistor(**s**) (Gi/Fi)
- Time consuming
- Depending on the design frequency :
  - bipolar
  - unipolar
- Starting from selection guides **recommended**
- Pt. 5 example

Step - 2

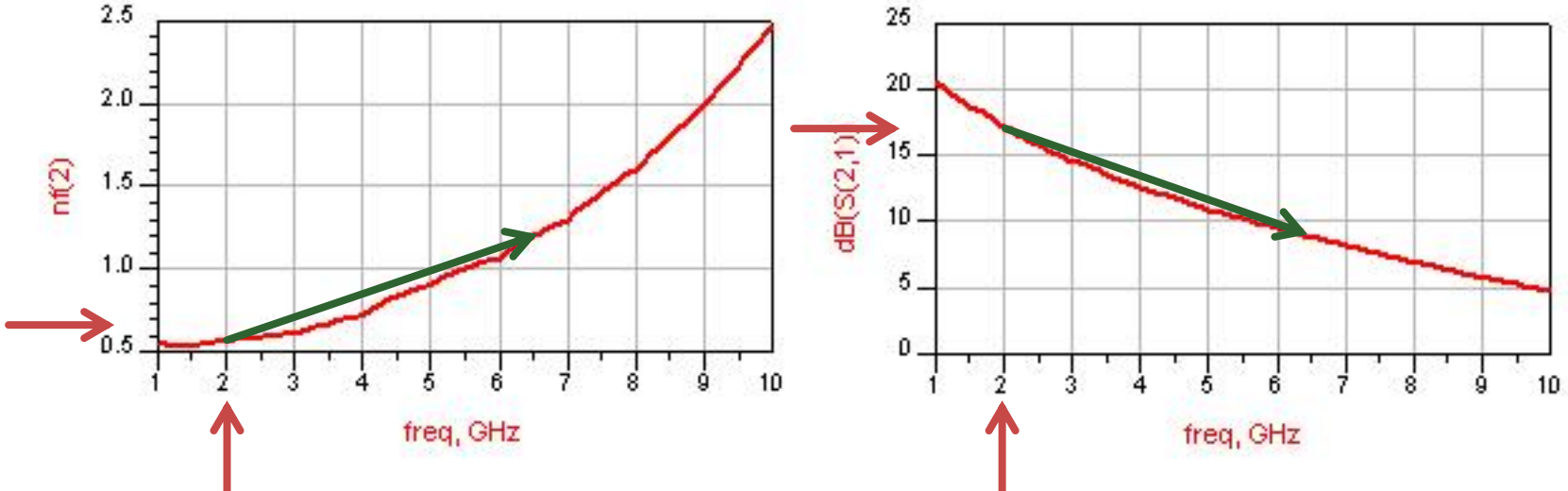
- Few selection guides available on rf-opto
- -> Google: microwave/rf transistor, low noise, LNA

Low Noise pHEMTs (Typical Specifications @ 25°C Case Temperature)

Part Number	Gate Width (µm)	Frequency Range (GHz)	Test Freq. (GHz)	V_{dd} (V)	I_{dd} (mA)	NF_o (dB)	G_a (dB)	OIP3 (dBm)	$P_{1\,dB}$ (dBm)	Package
ATF-33143	1600	0.45 - 6	2	4	80	0.5	15.0	33.5	+22	SOT-343 (SC-70)
ATF-331M4	1600	0.45 - 6	2	4	60	0.6	15.0	31	+19	MiniPak[2]
ATF-34143	800	0.45 - 6	2	4	60	0.5	17.5	31.5	+20	SOT-343 (SC-70)
ATF-35143	400	0.45 - 6	2	2	15	0.4	18.0	21	+10	SOT-343 (SC-70)
ATF-38143	800	0.45 - 6	2	2	10	0.4	16.0	22	+12	SOT-343 (SC-70)
ATF-36077	200	1.5 - 18	12	1.5	10	0.5	12.0	—	+5	70 mil SM
ATF-36163	200	1.5 - 18	12	1.5	15	1.2	10.0	—	+5	SOT-363 (SC-70)

Step - 2

- Take into account the typical variation of the parameters to estimate from test frequency to design frequency
  - Noise factor **increases** with increasing frequency
  - Gain **decreases** with increasing frequency

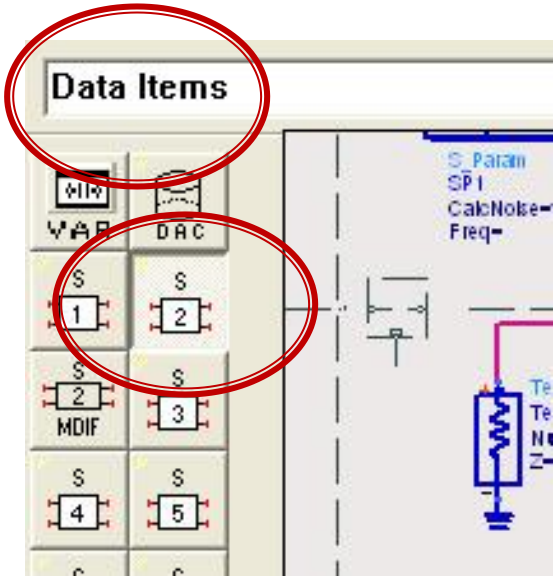


Step - 2

- Result
  - candidate T1: **ATF34143**
  - candidate T2: **NE71084**

Step - 3

- Obtain model data for the candidate transistor(**s**)
- Most often S parameter files (Touchstone)
- Google, manufacturer site: S2p files, S parameters etc.

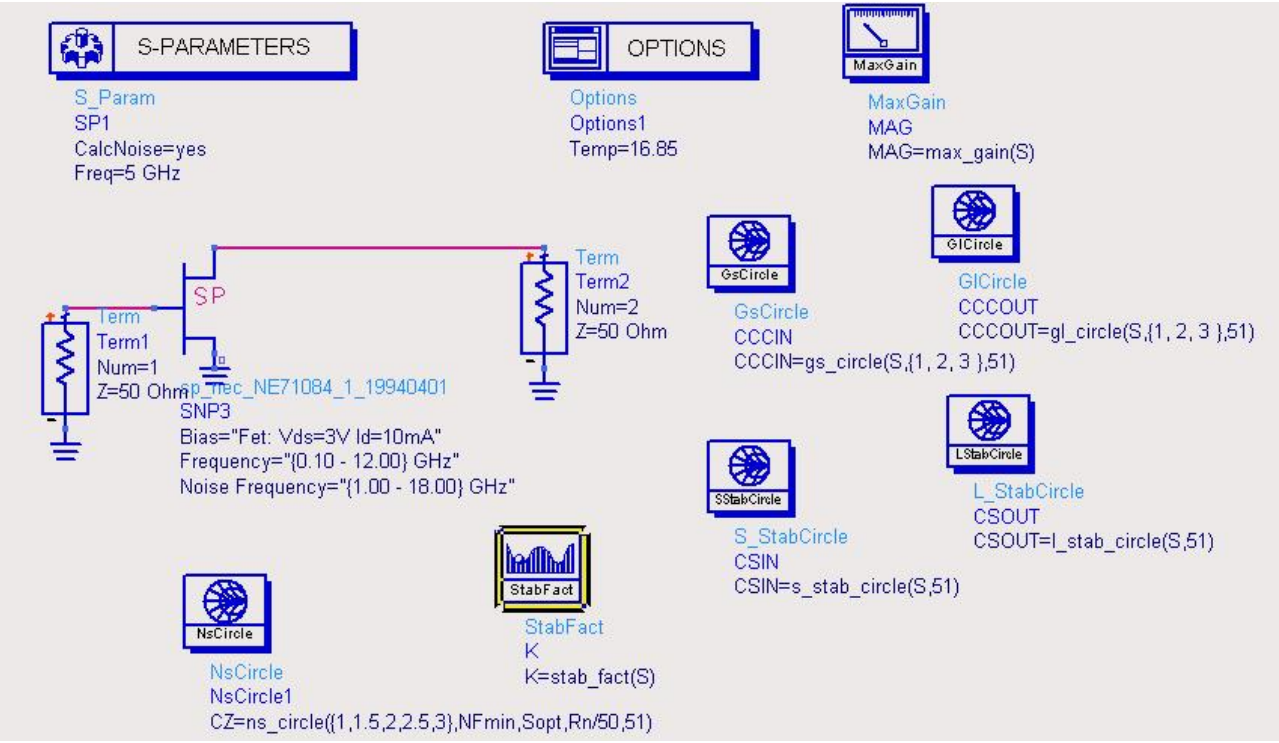


Step - 4

- Investigate the transistor
  - schematic 1/lab 3-4
  - compute some values (check G/F at design frequency)
  - compute some circles (position, diameter)
  - estimate/choose GS/GL
    - similar to lab3-4
    - for each transistor
- Pt. 7 example

Step - 4

- introduce a succession of multiple S parameter files and simulate (**repeatedly**)



Step - 4

- Result
  - candidate T1: **ATF34143 la 3V, 20mA, GS1 = ~ … dB, GL1 = ~ …dB**
  - candidate T2: **NE71084 la 3V, 1mA , GS2 = ~ … dB, GL2 = ~ …dB**

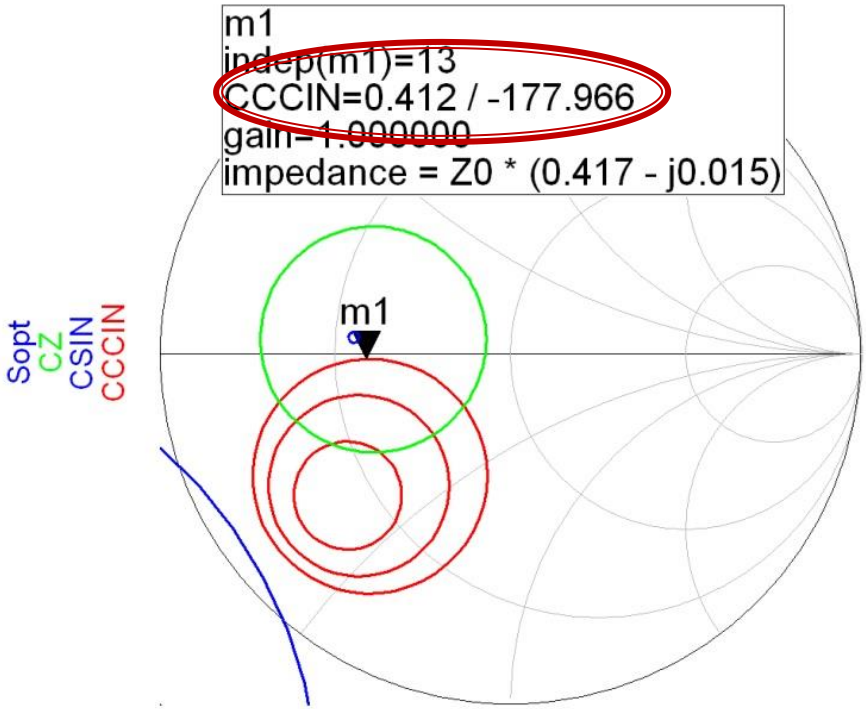
Step - 5

- For each transistor:
- Design of the input matching network
  - schematics 1~2/lab 3-4
- circles on the Smith Chart
  - stability circle
  - noise circle(**s**) (~chosen F)
  - gain circle(**s**) (~chosen GS)

- Pt. 8,9 example

Step - 5

- Use a marker to get the value of the reflection coefficient Γ_S
  - draw a dummy circle to have a point for the marker



Step - 5

- Calculate the electrical lengths of the two series/parallel lines according to the examples in the course/project
  - write down (on paper) the computation (**!!"andrei" factor**)

$$\cos(\varphi + 2\theta) = -|\Gamma_S|$$

$$\theta_{sp} = \beta \cdot l = \tan^{-1} \frac{\mp 2 \cdot |\Gamma_S|}{\sqrt{1 - |\Gamma_S|^2}}$$

Step - 5

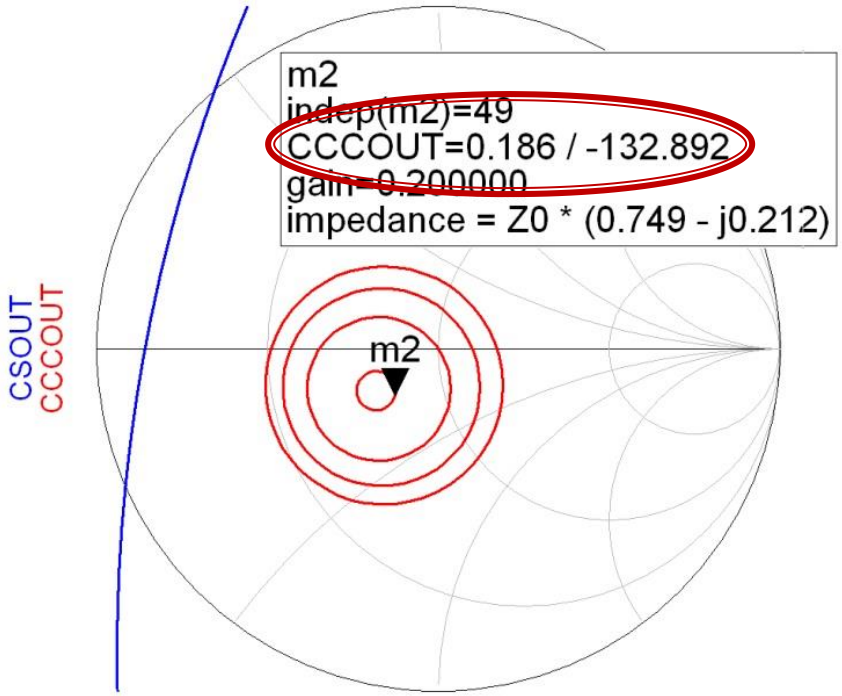
- Result:
  - electrical length **E1, E2**
  - for each transistor

Step - 6

- For each transistor:
- Design of the output matching network
  - schematics 1~2/lab 3-4
- circles on the Smith Chart
  - stability circle
  - ~~noise circle(**s**) (~chosen F)~~
  - gain circle(**s**) (~chosen GL)
- Pt. 8,9 example

Step - 6

- Use a marker to get the value of the reflection coefficient Γ_L



Step - 6

- Calculate the electrical lengths of the two series/parallel lines according to the examples in the course/project
  - write down (on paper) the computation (**!!"andrei" factor**)

$$\cos(\varphi + 2\theta) = -|\Gamma_L|$$

$$\theta_{sp} = \beta \cdot l = \tan^{-1} \frac{\mp 2 \cdot |\Gamma_L|}{\sqrt{1 - |\Gamma_L|^2}}$$

Step - 6

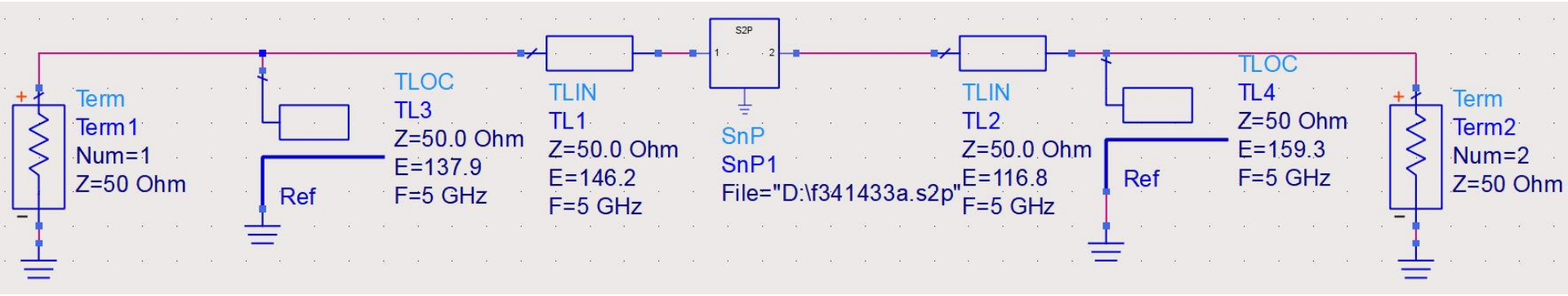
- Result:
  - electrical length **E_3, E_4**
  - for each transistor

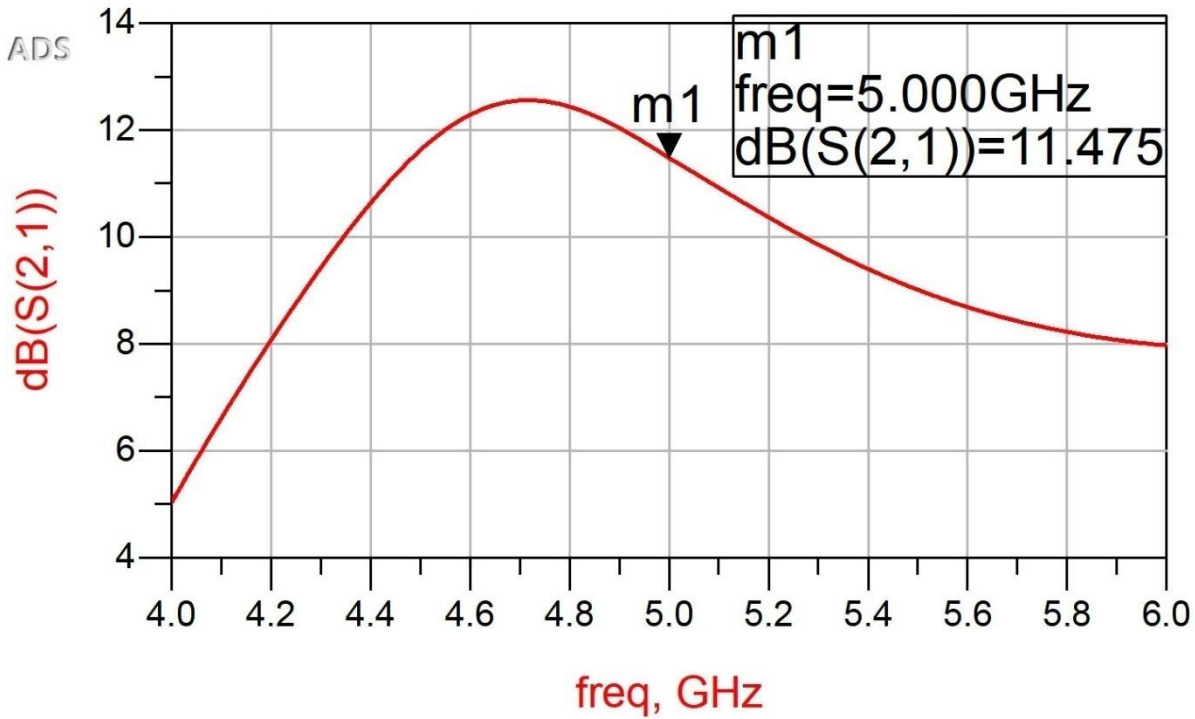
Step - 7

- For each transistor
- Check E1, E2, E3, E4
- Insert lines E1, E2 as the input network and E3, E4 as the output network and check if the proposed G / NF results are obtained.
  - Check and repeat the calculations

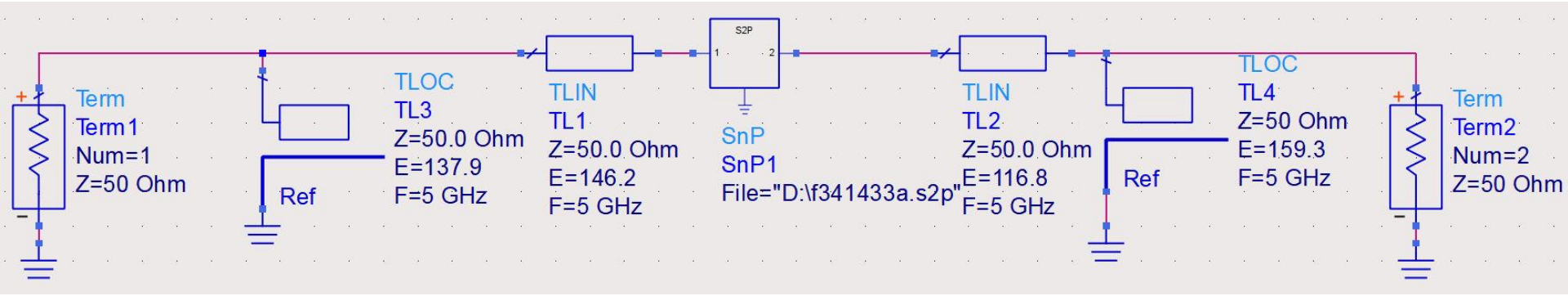
- Pt. 8,9 example

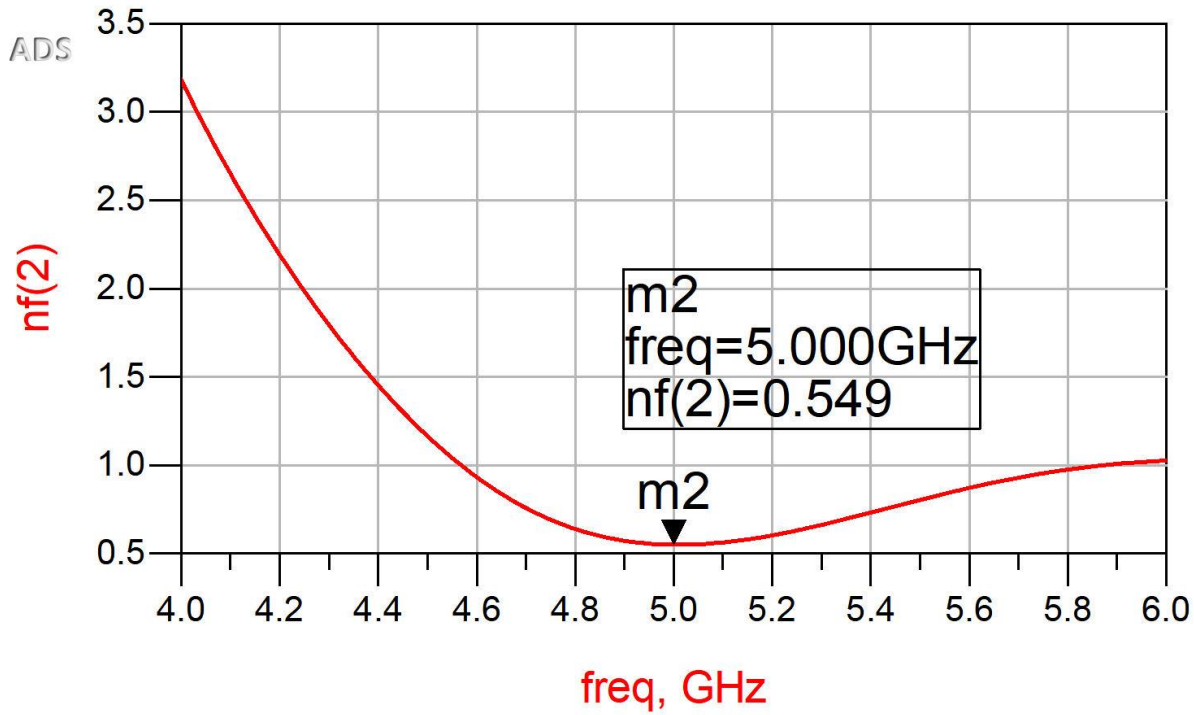
Step - 7


Term
Term1
Num=1
Z=50 Ohm
Ref
TLOC
TL3
Z=50.0 Ohm
E=137.9
F=5 GHz
TLIN
TL1
Z=50.0 Ohm
E=146.2
F=5 GHz
S2P
1
2
SnP
SnP1
File="D:\f341433a.s2p"
TLIN
TL2
Z=50.0 Ohm
E=116.8
F=5 GHz
Ref
TLOC
TL4
Z=50 Ohm
E=159.3
F=5 GHz
Term
Term2
Num=2
Z=50 Ohm


ADS
m1
freq=5.000GHz
dB(S(2,1))=11.475
dB(S(2,1))
freq, GHz
14
12
10
8
6
4
4.0
4.2
4.4
4.6
4.8
5.0
5.2
5.4
5.6
5.8
6.0

Step - 7


Term
Term1
Num=1
Z=50 Ohm
Ref
TLOC
TL3
Z=50.0 Ohm
E=137.9
F=5 GHz
TLIN
TL1
Z=50.0 Ohm
E=146.2
F=5 GHz
S2P
1
2
SnP
SnP1
File="D:\f341433a.s2p"
TLIN
TL2
Z=50.0 Ohm
E=116.8
F=5 GHz
Ref
TLOC
TL4
Z=50 Ohm
E=159.3
F=5 GHz
Term
Term2
Num=2
Z=50 Ohm


ADS
nf(2)
3.5
3.0
2.5
2.0
1.5
1.0
0.5
4.0
4.2
4.4
4.6
4.8
5.0
5.2
5.4
5.6
5.8
6.0
m2
freq=5.000GHz
nf(2)=0.549
m2
freq, GHz

Step - 7

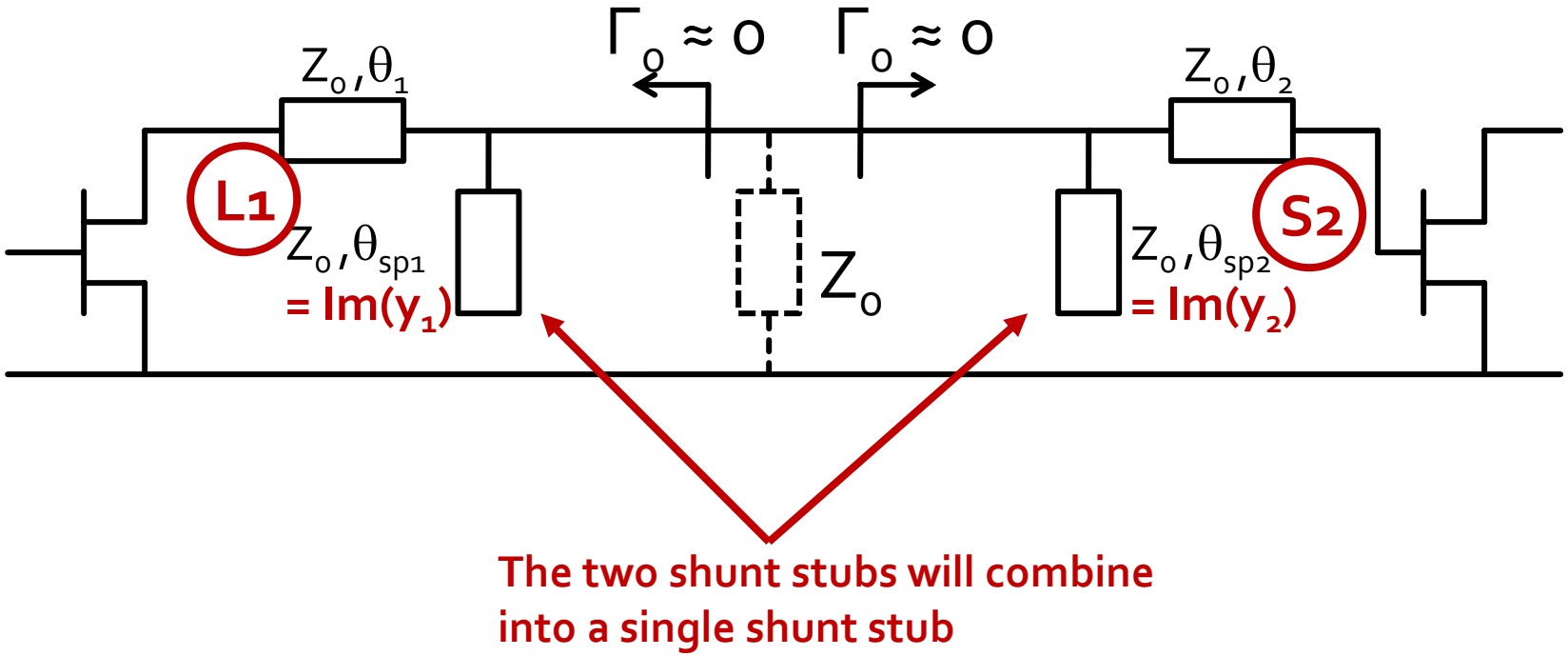
- Result
  - adopted T1: **ATF34143 la 3V, 20mA, GS1 = … dB, GL1 = …dB**
  - adopted T2: **NE71084 la 3V, 1mA , GS2 = … dB, GL2 = …dB**

Step - 8

- Following steps 1-7 we have two functional one transistor amplifier stages which fulfill Friis formulae:
  - G_1, G_2 $\quad G_{cas} = G_1 \cdot G_2 \qquad G_{cas}[dB] = G_{tema} + \Delta G$
  - F_1, F_2 $\quad F_{cas} = F_1 + \frac{1}{G_1}(F_2 - 1) \qquad F_{cas}[dB] = F_{tema} - \Delta F$
- Cascade connection of the two amplifiers to get a single two stage amplifier
- Pt. 10 example

Step - 8

- Following steps 5,6 we know the electrical lengths of the lines from the output of first transistor and input of the second transistor

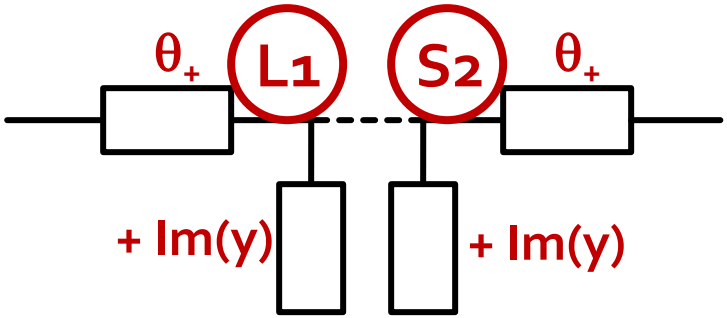


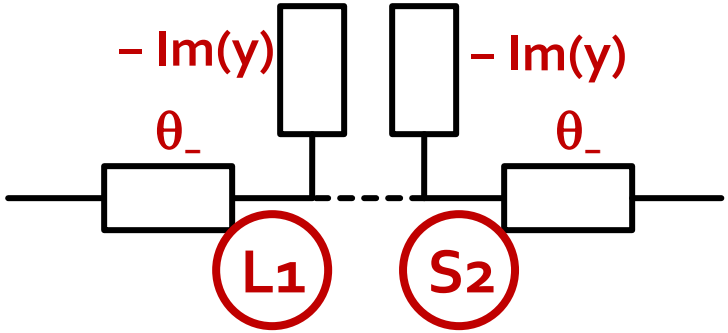
Step - 8

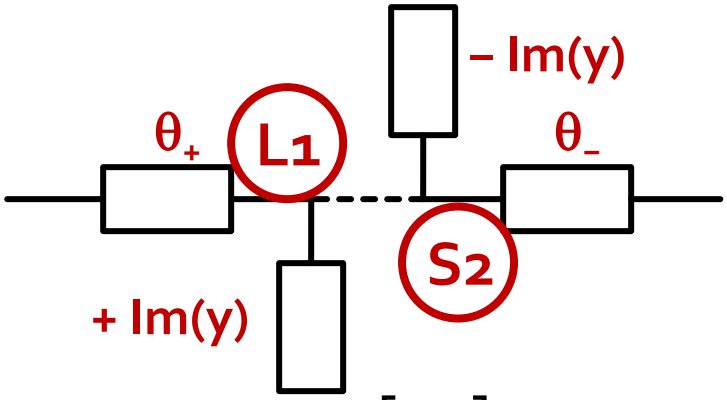
- The two series lines keep their previous values
  - **Attention!** solutions are dual +/- for both amplifiers, for every series line any of the two solutions are available (**independently**)
- The two shunt lines combine into a single shunt line
  - **Attention!** admittances are in parallel and add up, not the electrical lengths
  - Recovering $Im(y_1)$, $Im(y_2)$ from step 5,6 computations is required
  - Solutions for admittances are also dual, chose (+/-) values corresponding to **already chosen solutions** for the series lines

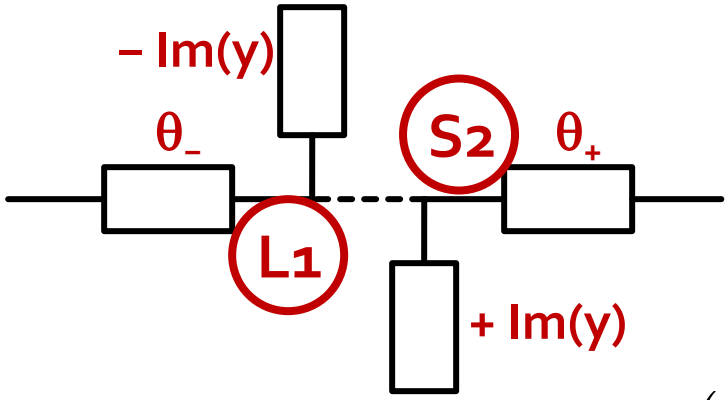
Step - 8

- 4 possible combinations
  - **admittances** are in parallel and **add up**, not the electrical lengths









$$\mathrm{Im}\left[y_{sp}\right] = \mathrm{Im}\left[y_{L1}(\theta)\right] + \mathrm{Im}\left[y_{S2}(\theta)\right]$$

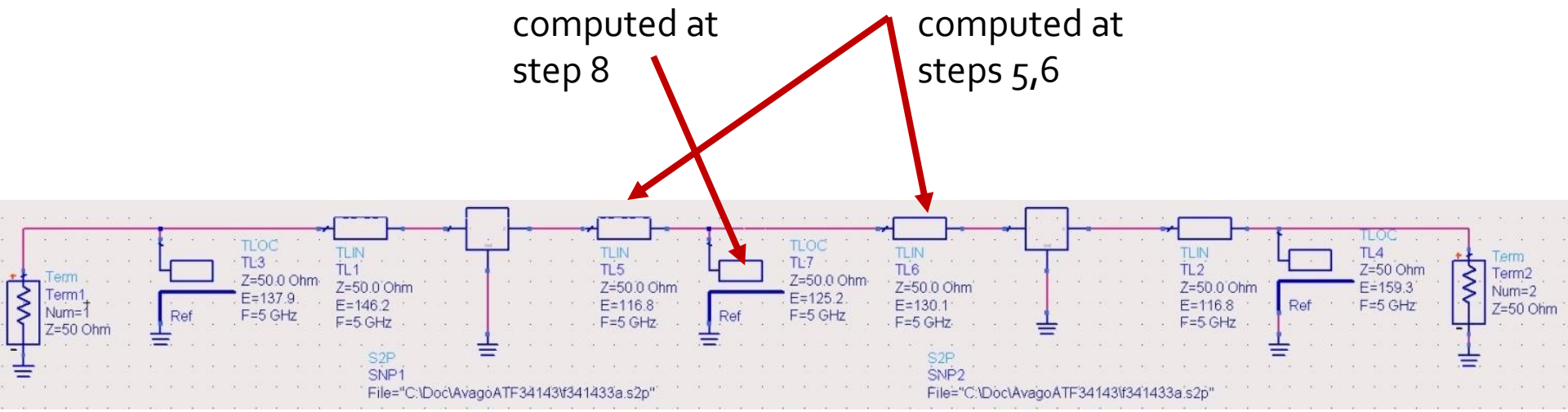
$$\theta_{sp} = \tan^{-1}\left(\mathrm{Im}\left[y_{sp}\right]\right)$$

Step - 8

- Compute the required admittance of the combined shunt stub
  - $Im(y) = Im(y_1) + Im(y_2)$
- Compute the electrical length that offer this admittance
  - $E = \tan^{-1}(Im(y))$
- Combine the two amplifiers, keeping the series lines and replacing the interstage shunt stubs with the computed combined shunt stub

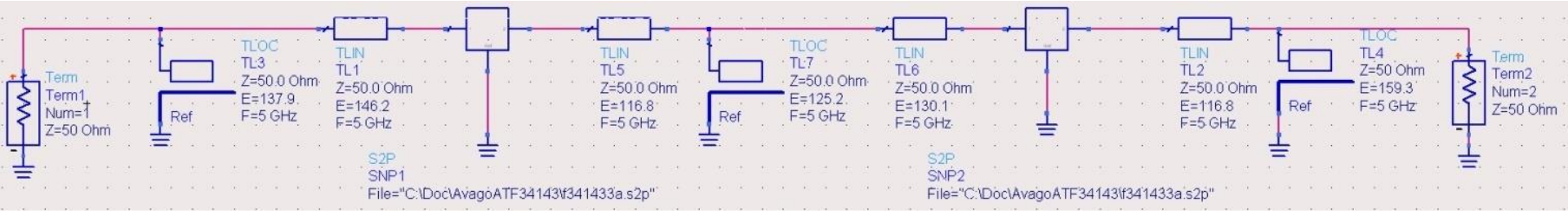
Step - 8

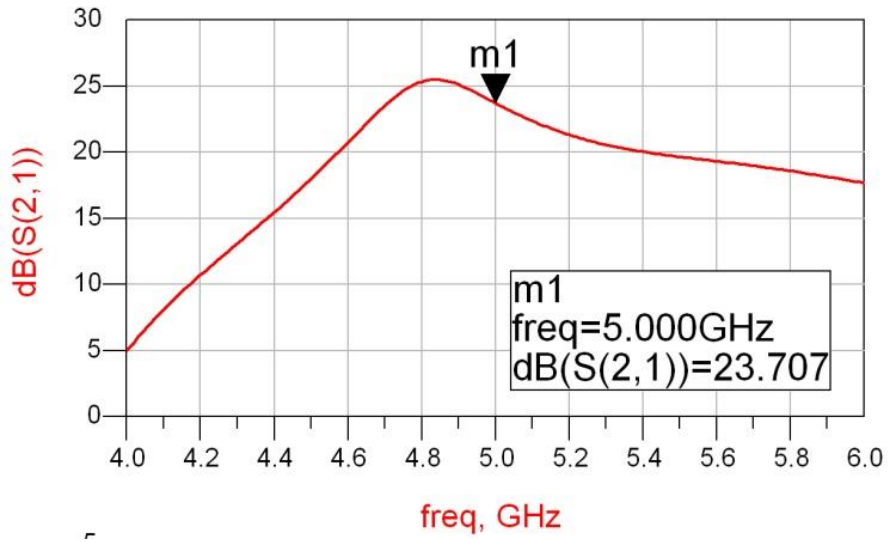
- Result
  - final amplifier
- Simulate to verify computations
  - Pt. 11 example

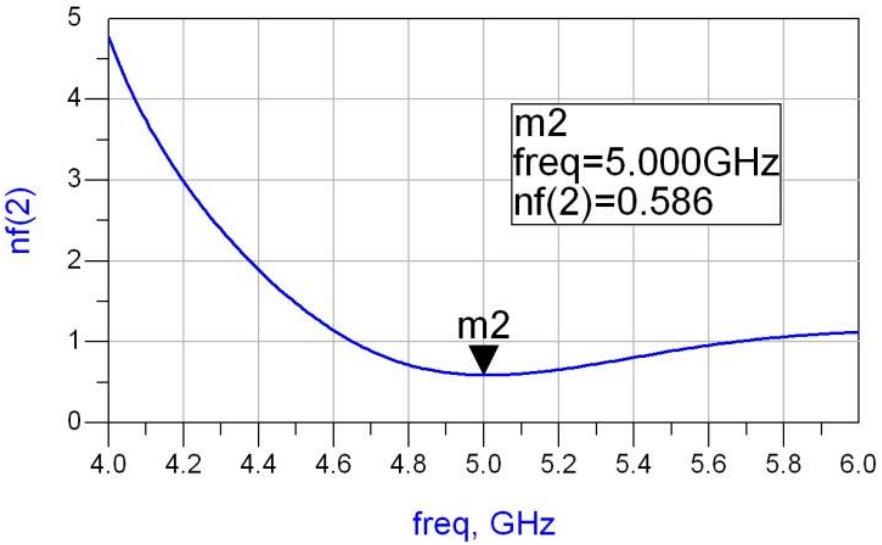


Step - 8

- Simulate to verify computations







Step - 9

- Design and draw filter schematic
- Pt. 13 example

- Depending on the type of filter formulae and schematic are different
  - other type other than coupled-lines offers bonus point

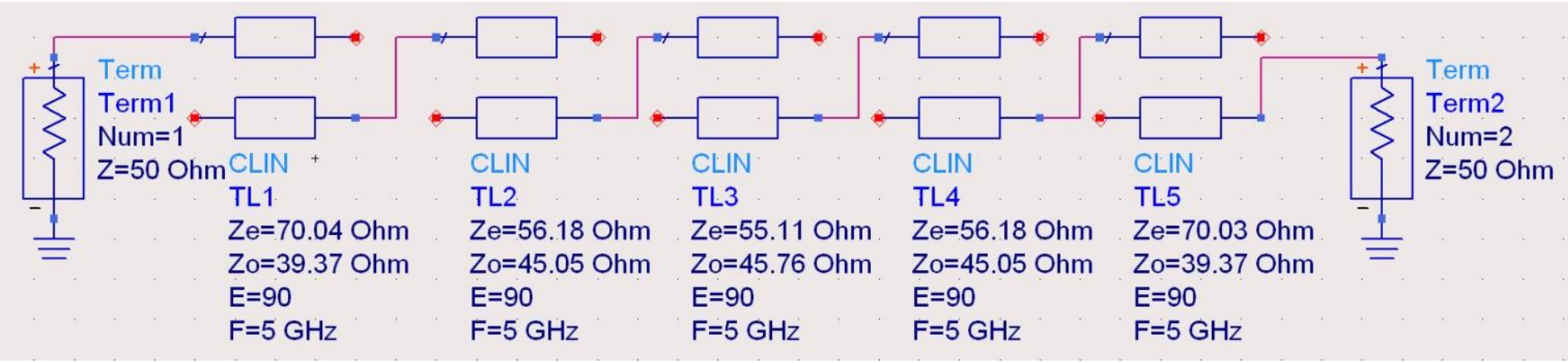
Step - 9

- **Attention!** Filter design can be done only by computation
  - due to high number of parameters (order 5-6, 12-14 parameters) **it's not possible** to get good results by tuning

n	g_n	$Z_o J_n$	Z_{oe} [Ω]	Z_{oo} [Ω]
1	1.6703	0.306664	70.04	39.37
2	1.1926	0.111295	56.18	45.05
3	2.3661	0.09351	55.11	45.76
4	0.8419	0.111294	56.18	45.05
5	1.9841	0.306653	70.03	39.37

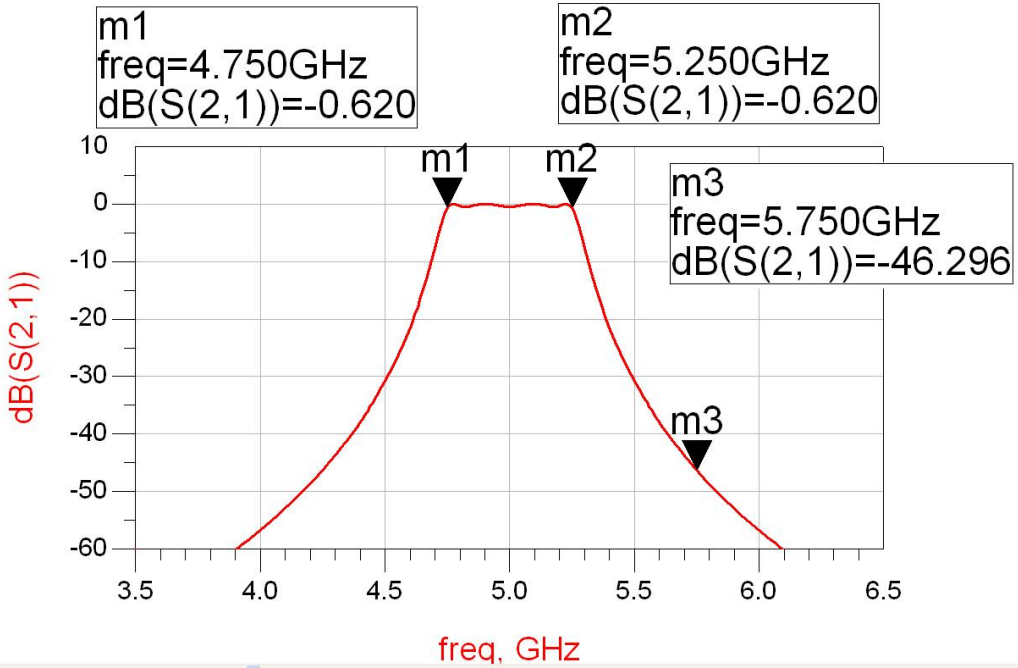
Step - 9

- Simulate to verify filter separately



Step - 9

- Check carefully the passband, and maximum ripple/loss in passband
  - correct passband is **significant** in project grade
  - eventual uncontrolled losses in passband will lower amplifier gain and gain assignment fulfillment might fail



Step - 10

- Follow lab 3 principles for final tune
  - input lines mainly to change noise, output lines only change gain
- Pt. 14 example

Step - 11

- Implement supplemental design for additional points
  - Proving additional points will require submission of archived ADS project (*.zap)

Contact

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